

COMPAL CONFIDENTIAL

MODEL NAME : ADP80/81

PCB NO : LA-C841P

BOM P/N : 4319YK31LXX

GPIO MAP: Gen7 GPIO Master_0115

Park City 15" H DSC

Skylake H

2015-09-08

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

TB@ : AR TBT Component

DIS@ : GPU Component

UMA@ : UMA Component


Litho@ : GPU Litho Component

Tropo@ : GPU Tropo Component

H/P Check RE300

MB PCB	
Part Number	Description
D421E000101	PCB ADP80 LA-C841P LS-C641P


Layout Dell logo



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REV: A00
PWB:

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Title

Cover Sheet

Size Document Number

Rev 0.1

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN	+3.3V_M +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA	(M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	TU662	0.5
			Add Plating		
1	Top	3.7	Copper foil	0.5oz+plating	1.8
			Prepreg	1080	1.8
2	GND	3.7	Copper foil	1oz	1.25
			Core	4mil	3.97
3	IN 1	3.7	Copper foil	1oz	1.25
			Prepreg	2116H	1.4
4	GND.PWR	3.7	Copper foil	1oz	1.25
			Core	4mil	3.97
5	IN 2	3.7	Copper foil	1oz	1.25
			Prepreg	1080H x2	1.4
6	IN 3	3.7	Copper foil	1oz	1.25
			Core	4mil	3.97
7	GND.PWR	3.7	Copper foil	1oz	1.25
			Prepreg	2116H	1.4
8	IN 4	3.7	Copper foil	1oz	1.25
			Core	4mil	3.97
9	GND	3.7	Copper foil	1oz	1.25
			Prepreg	1080	1.8
10	Bottom	3.7	Copper foil	0.5oz+plating	1.8
			Add Plating		
			SolderMask	TU662	0.5
Overall Thickness (1.2mm ± 10%)					48.28000 1.226312

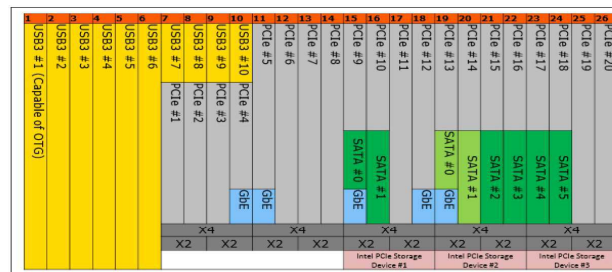
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right up
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB1-->Right down
USB3.0-4				JUSB2-->Rear
USB3.0-5				NA
USB3.0-6				EDOCK
USB3.0-7		PCIE-1		JNGFF1-->M.2 3030(WIGIG)
USB3.0-8		PCIE-2		JNGFF1-->M.2 3030(WLAN)
USB3.0-9		PCIE-3		Card Reader
USB3.0-10		PCIE-4		LOM
		PCIE-5		Alpine Ridge - SP (pop only on Precision SKU)
		PCIE-6		
		PCIE-7		
		PCIE-8		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-9	SATA-0A	
		PCIE-10	SATA-1A	
		PCIE-11		
		PCIE-12		
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	EDOCK E-SATA
		PCIE-17	SATA-4	NA
		PCIE-18	SATA-5	NA
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB3-->Right up
2	JUSB1-->Right down
3	JUSB2 ->Rear
4	NA
5	EDOCK Port B
6	JNGFF1--> M.2 3030(BT)
7	EDOCK Port A
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera

USH	0	BIO
	1	NA

Check

VIDEO		DESTINATION
eDP		LCD
DDI-C	DeMux 1	M.2 3030 (WiGig)
		EDOCK Port B
		Alpine Ridge - SP (pop only on Precision SKU)
DDI-B	DeMux 2	EDOCK Port A
		JHDMI1
DDI-D	CONV VGA SW	MB VGA
		DOCK VGA



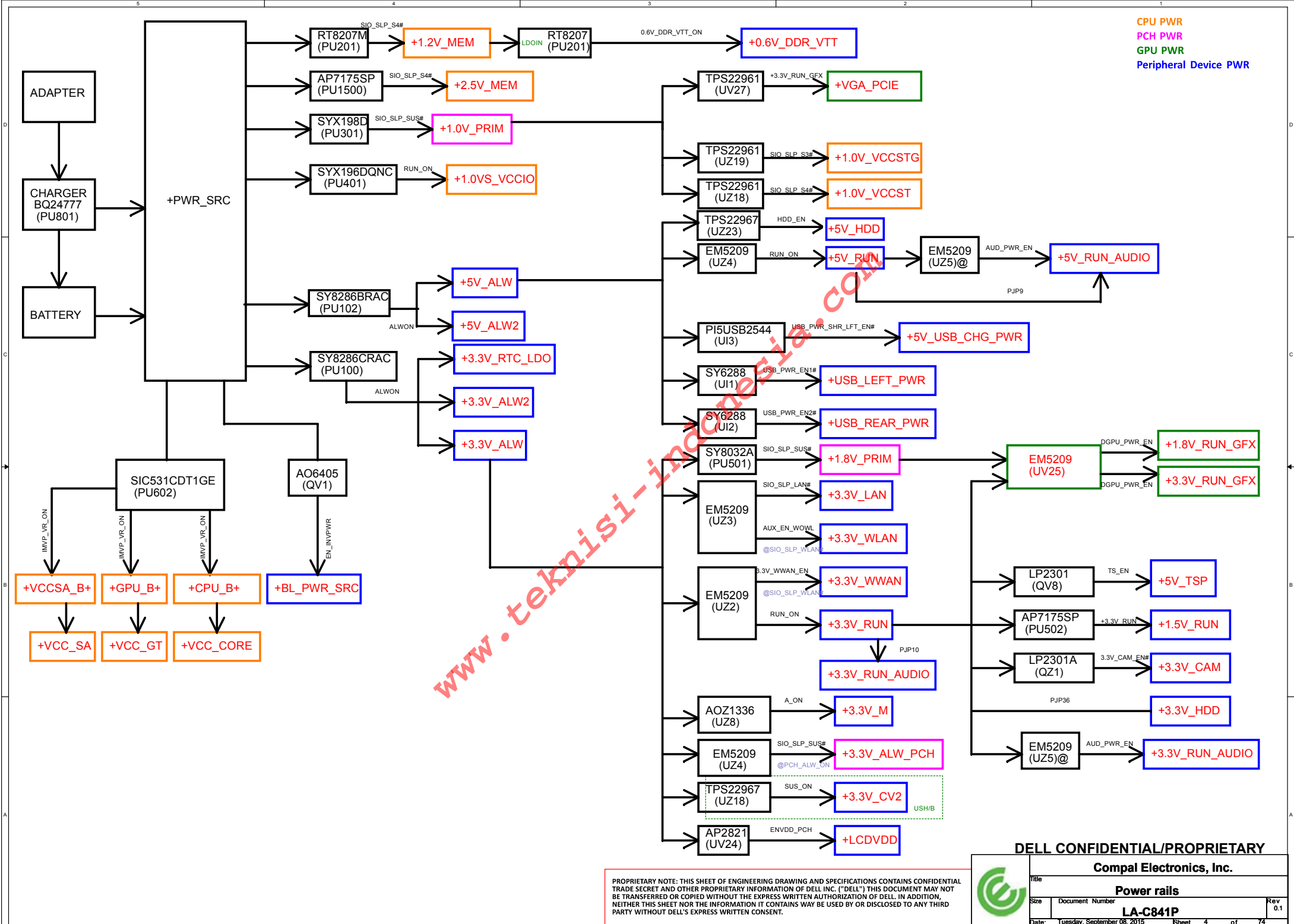
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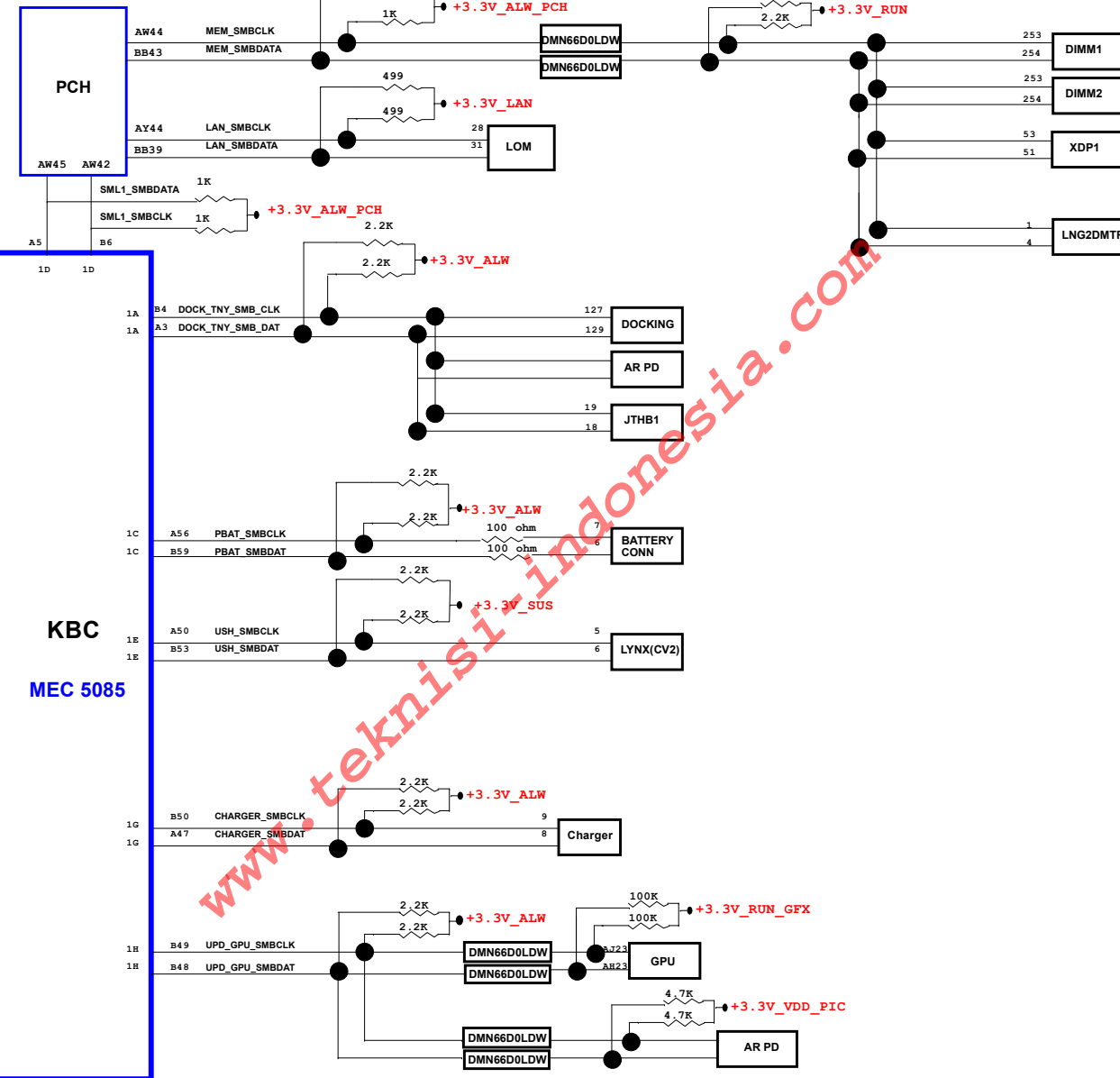
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SMBUS Address [0x9a]



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SMBus Block diagram

LA-C841P

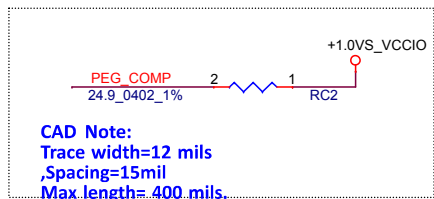
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PEG_CRX_GTX_N[0..15] <<PEG_CRX_GTX_N[0..15] <50>
PEG_CTX_C_GRX_P[0..15] >>PEG_CTX_C_GRX_P[0..15] <50>
PEG_CTX_C_GRX_N[0..15] >>PEG_CTX_C_GRX_N[0..15] <50>


		CPU1C SKYLAKE_HALO			
		BGA1440			
PEG_CRX_GTX_P15	E25	PEG_RXP[0]	PEG_TXP[0]	B25 PEG_CTX_GRX_P15Tropo@CC67 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P15
PEG_CRX_GTX_N15	D25	PEG_RXN[0]	PEG_TXN[0]	A25 PEG_CTX_GRX_N15Tropo@CC44 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N15
PEG_CRX_GTX_P14	E24	PEG_RXP[1]	PEG_TXP[1]	B24 PEG_CTX_GRX_P14Tropo@CC68 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P14
PEG_CRX_GTX_N14	F24	PEG_RXN[1]	PEG_TXN[1]	C24 PEG_CTX_GRX_N14Tropo@CC45 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N14
PEG_CRX_GTX_P13	E23	PEG_RXP[2]	PEG_TXP[2]	B23 PEG_CTX_GRX_P13Tropo@CC51 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P13
PEG_CRX_GTX_N13	D23	PEG_RXN[2]	PEG_TXN[2]	A23 PEG_CTX_GRX_N13Tropo@CC53 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N13
PEG_CRX_GTX_P12	E22	PEG_RXP[3]	PEG_TXP[3]	B22 PEG_CTX_GRX_P12Tropo@CC52 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P12
PEG_CRX_GTX_N12	F22	PEG_RXN[3]	PEG_TXN[3]	C22 PEG_CTX_GRX_N12Tropo@CC73 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N12
PEG_CRX_GTX_P11	E21	PEG_RXP[4]	PEG_TXP[4]	B21 PEG_CTX_GRX_P11Tropo@CC69 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P11
PEG_CRX_GTX_N11	D21	PEG_RXN[4]	PEG_TXN[4]	A21 PEG_CTX_GRX_N11Tropo@CC46 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N11
PEG_CRX_GTX_P10	E20	PEG_RXP[5]	PEG_TXP[5]	B20 PEG_CTX_GRX_P10Tropo@CC54 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P10
PEG_CRX_GTX_N10	F20	PEG_RXN[5]	PEG_TXN[5]	C20 PEG_CTX_GRX_N10Tropo@CC74 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N10
PEG_CRX_GTX_P9	E19	PEG_RXP[6]	PEG_TXP[6]	B19 PEG_CTX_GRX_P9 Tropo@CC55 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P9
PEG_CRX_GTX_N9	D19	PEG_RXN[6]	PEG_TXN[6]	A19 PEG_CTX_GRX_N9 Tropo@CC47 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N9
PEG_CRX_GTX_P8	E18	PEG_RXP[7]	PEG_TXP[7]	B18 PEG_CTX_GRX_P8 Tropo@CC70 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P8
PEG_CRX_GTX_N8	F18	PEG_RXN[7]	PEG_TXN[7]	C18 PEG_CTX_GRX_N8 Tropo@CC56 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N8
PEG_CRX_GTX_P7	D17	PEG_RXP[8]	PEG_TXP[8]	A17 PEG_CTX_GRX_P7 DIS@ CC57 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P7
PEG_CRX_GTX_N7	E17	PEG_RXN[8]	PEG_TXN[8]	B17 PEG_CTX_GRX_N7 DIS@ CC75 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N7
PEG_CRX_GTX_P6	F16	PEG_RXP[9]	PEG_TXP[9]	C16 PEG_CTX_GRX_P6 DIS@ CC58 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P6
PEG_CRX_GTX_N6	E16	PEG_RXN[9]	PEG_TXN[9]	B16 PEG_CTX_GRX_N6 DIS@ CC48 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N6
PEG_CRX_GTX_P5	D15	PEG_RXP[10]	PEG_TXP[10]	A15 PEG_CTX_GRX_P5 DIS@ CC71 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P5
PEG_CRX_GTX_N5	E15	PEG_RXN[10]	PEG_TXN[10]	B15 PEG_CTX_GRX_N5 DIS@ CC59 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N5
PEG_CRX_GTX_P4	F14	PEG_RXP[11]	PEG_TXP[11]	C14 PEG_CTX_GRX_P4 DIS@ CC60 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P4
PEG_CRX_GTX_N4	E14	PEG_RXN[11]	PEG_TXN[11]	B14 PEG_CTX_GRX_N4 DIS@ CC76 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N4
PEG_CRX_GTX_P3	D13	PEG_RXP[12]	PEG_TXP[12]	A13 PEG_CTX_GRX_P3 DIS@ CC61 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P3
PEG_CRX_GTX_N3	E13	PEG_RXN[12]	PEG_TXN[12]	B13 PEG_CTX_GRX_N3 DIS@ CC49 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N3
PEG_CRX_GTX_P2	F12	PEG_RXP[13]	PEG_TXP[13]	C12 PEG_CTX_GRX_P2 DIS@ CC72 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P2
PEG_CRX_GTX_N2	E12	PEG_RXN[13]	PEG_TXN[13]	B12 PEG_CTX_GRX_N2 DIS@ CC62 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N2
PEG_CRX_GTX_P1	D11	PEG_RXP[14]	PEG_TXP[14]	A11 PEG_CTX_GRX_P1 DIS@ CC63 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P1
PEG_CRX_GTX_N1	E11	PEG_RXN[14]	PEG_TXN[14]	B11 PEG_CTX_GRX_N1 DIS@ CC77 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N1
PEG_CRX_GTX_P0	F10	PEG_RXP[15]	PEG_TXP[15]	C10 PEG_CTX_GRX_P0 DIS@ CC64 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_P0
PEG_CRX_GTX_N0	E10	PEG_RXN[15]	PEG_TXN[15]	B10 PEG_CTX_GRX_N0 DIS@ CC50 2	1 0.22U 0402 10V6K PEG_CTX_C_GRX_N0

		PEG_COMP G2		PEG_RCOMP	
<17> DMI_CRX_PTX_P0	D8	DMI_RXP[0]	DMI_TXP[0]	B8 DMI_CTX_PRX_P0	<17> DMI_CTX_PRX_P0
<17> DMI_CRX_PTX_N0	E8	DMI_RXN[0]	DMI_TXN[0]	A8 DMI_CTX_PRX_N0	<17> DMI_CTX_PRX_N0
<17> DMI_CRX_PTX_P1	E6	DMI_RXP[1]	DMI_TXP[1]	C6 DMI_CTX_PRX_P1	<17> DMI_CTX_PRX_P1
<17> DMI_CRX_PTX_N1	F6	DMI_RXN[1]	DMI_TXN[1]	B6 DMI_CTX_PRX_N1	<17> DMI_CTX_PRX_N1
<17> DMI_CRX_PTX_P2	D5	DMI_RXP[2]	DMI_TXP[2]	B5 DMI_CTX_PRX_P2	<17> DMI_CTX_PRX_P2
<17> DMI_CRX_PTX_N2	E5	DMI_RXN[2]	DMI_TXN[2]	A5 DMI_CTX_PRX_N2	<17> DMI_CTX_PRX_N2
<17> DMI_CRX_PTX_P3	J8	DMI_RXP[3]	DMI_TXP[3]	D4 DMI_CTX_PRX_P3	<17> DMI_CTX_PRX_P3
<17> DMI_CRX_PTX_N3	J9	DMI_RXN[3]	DMI_TXN[3]	B4 DMI_CTX_PRX_N3	<17> DMI_CTX_PRX_N3

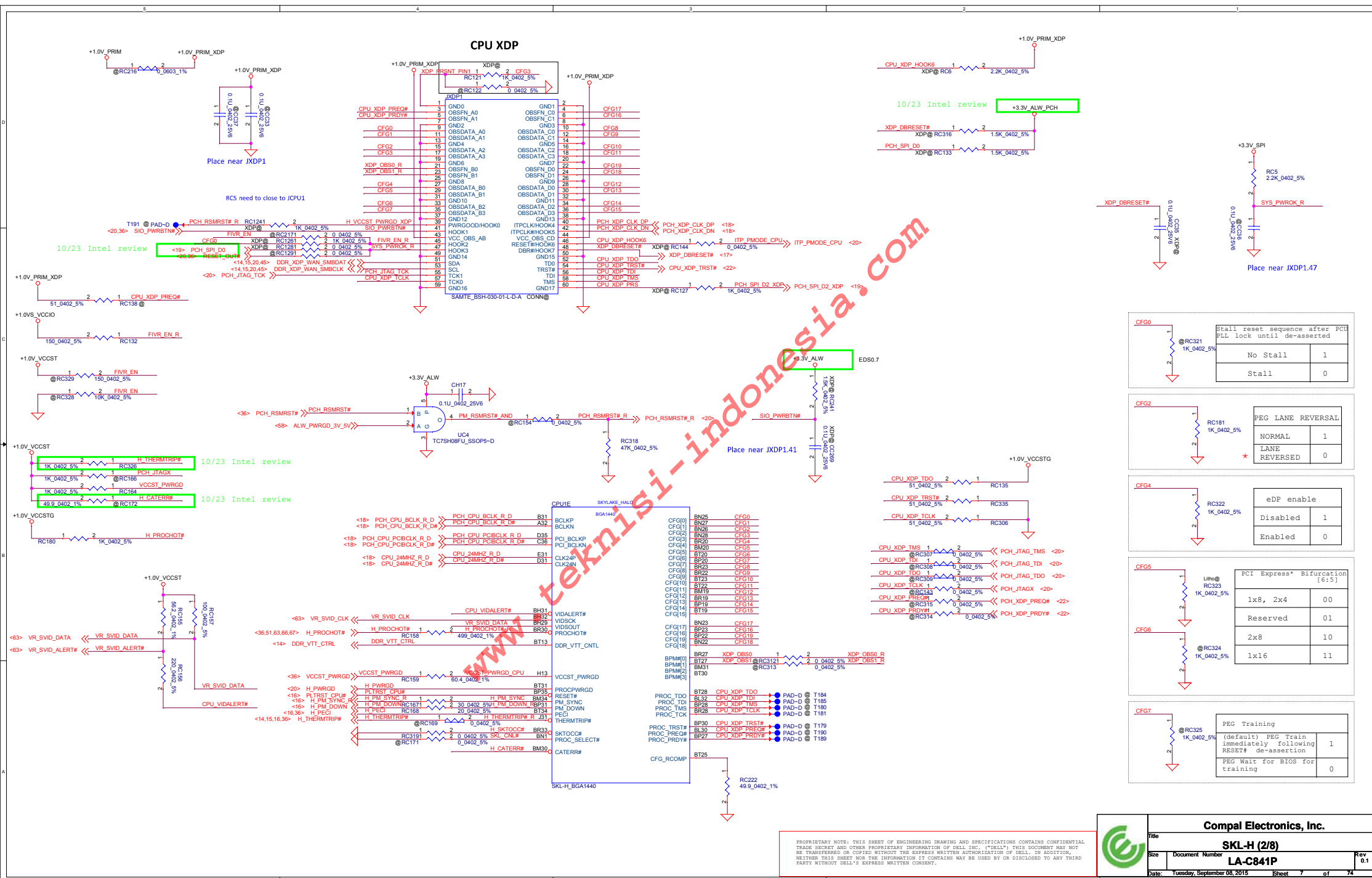


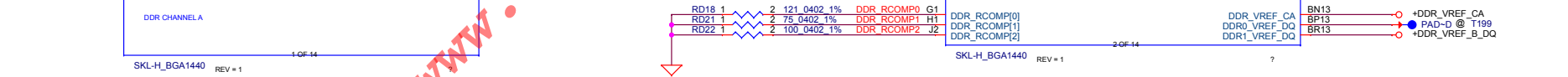
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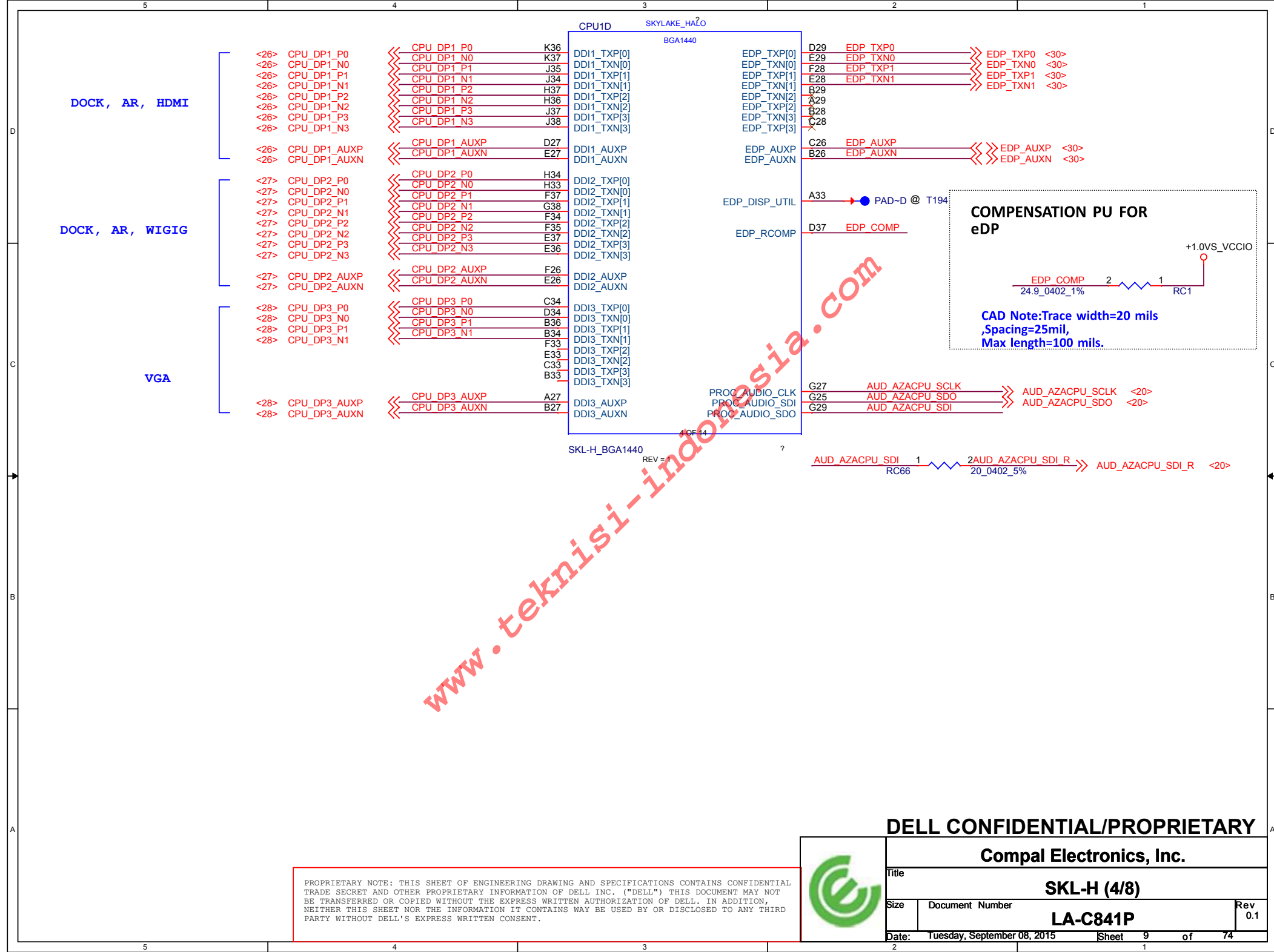


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The diagram shows four signals on the left and two clock signals on the right. The signals are DDR_A_D[0.63], DDR_B_D[0.63], DDR_A_CB[0.7], and DDR_B_CB[0.7]. The clock signals are DDR_A_DQS#[0.8] and DDR_B_DQS#[0.8]. The signals are shown as blue lines with red markers indicating specific time points. The clock signals are shown as blue lines with red markers indicating specific time points.



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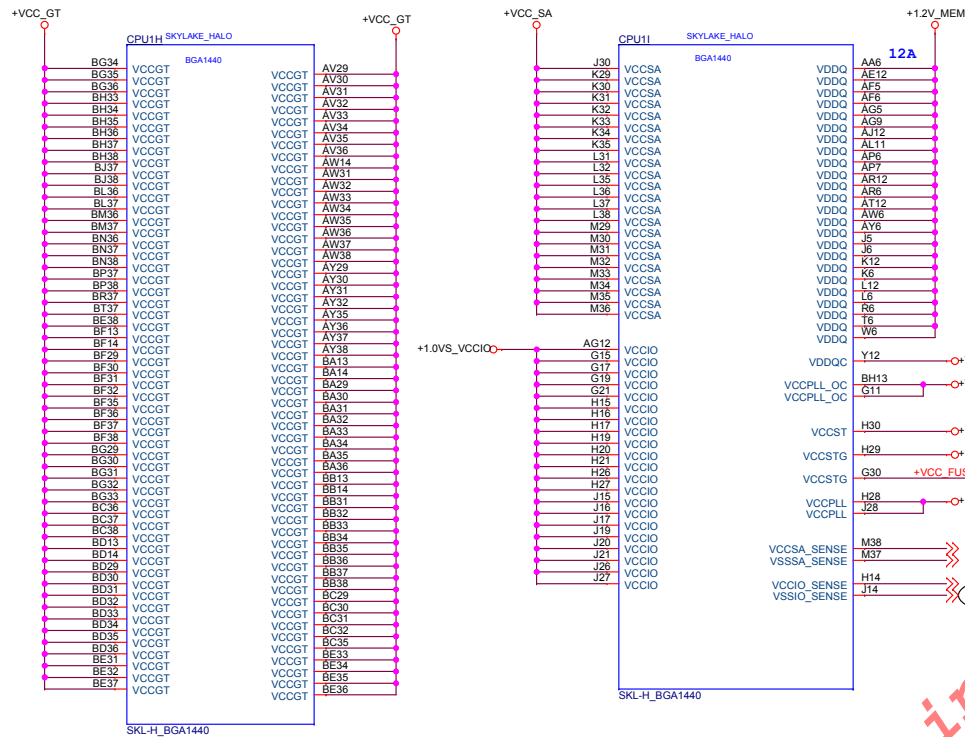
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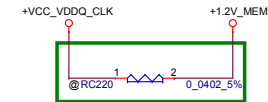
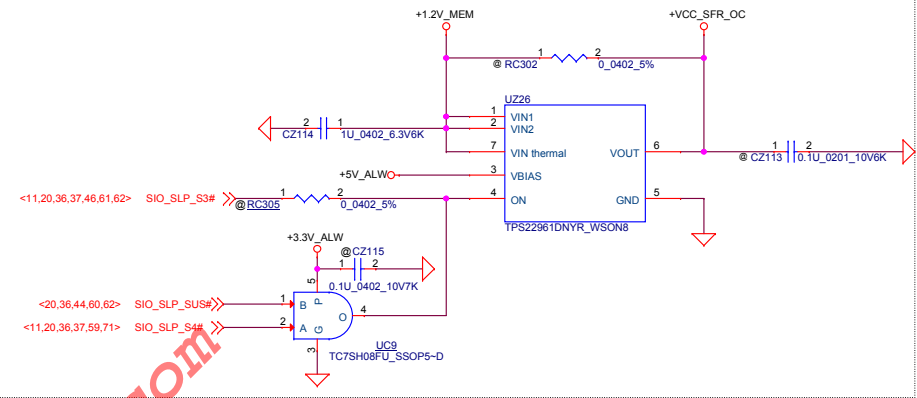
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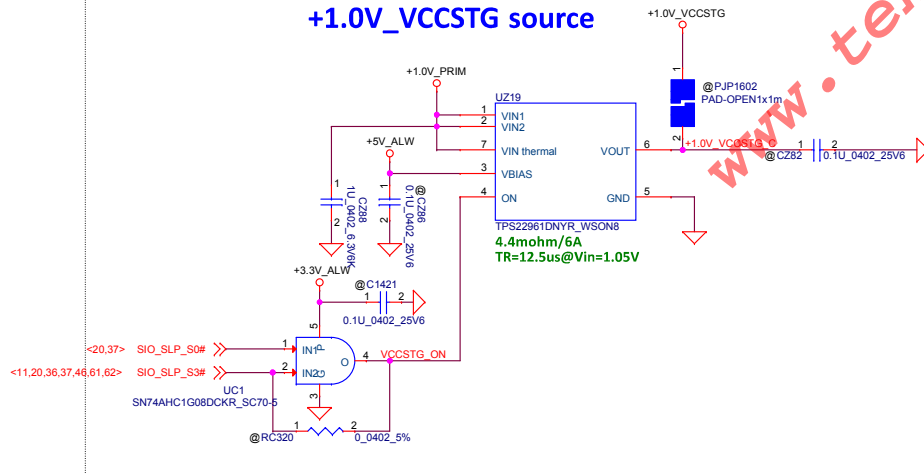
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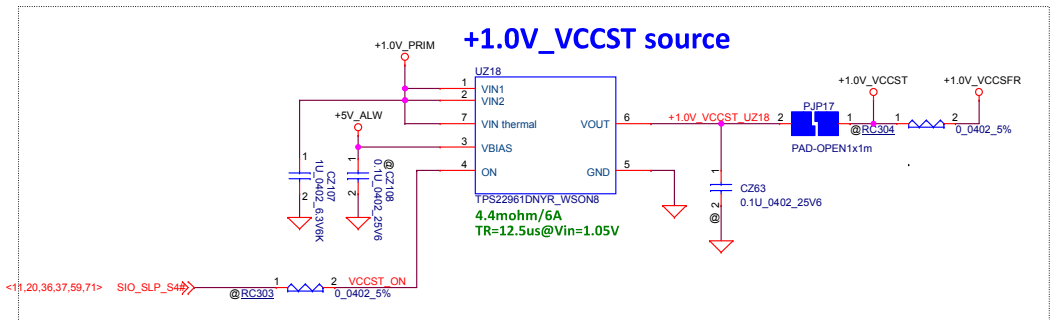
+VCCPLL_OC source



+1.0V_VCCSTG source



+1.0V_VCCST source



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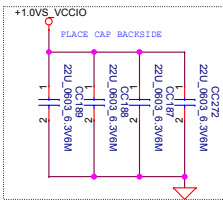
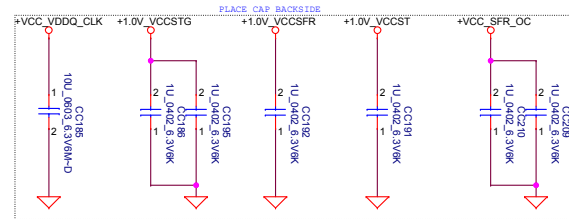
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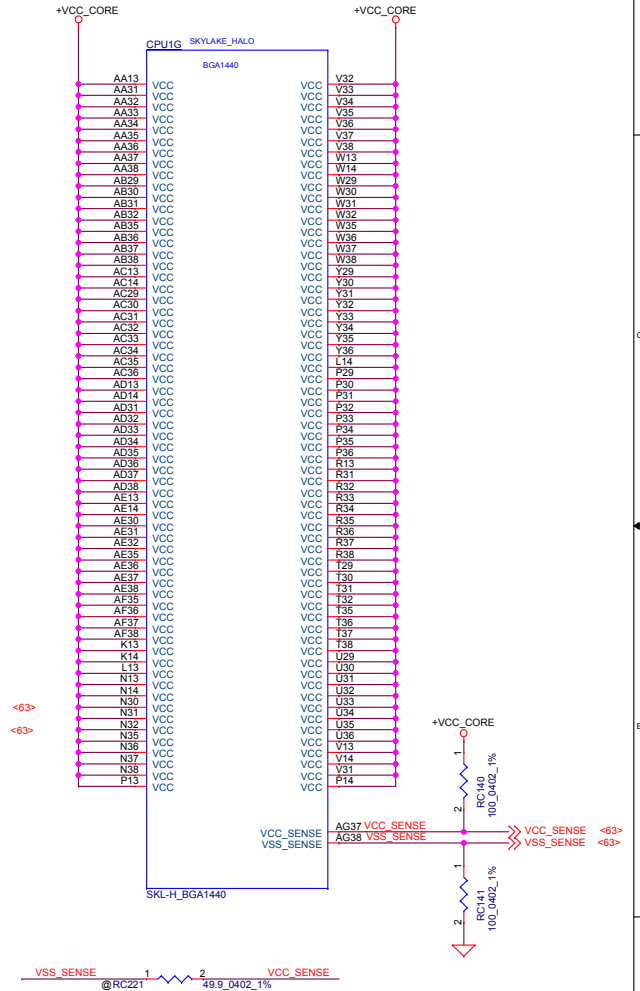
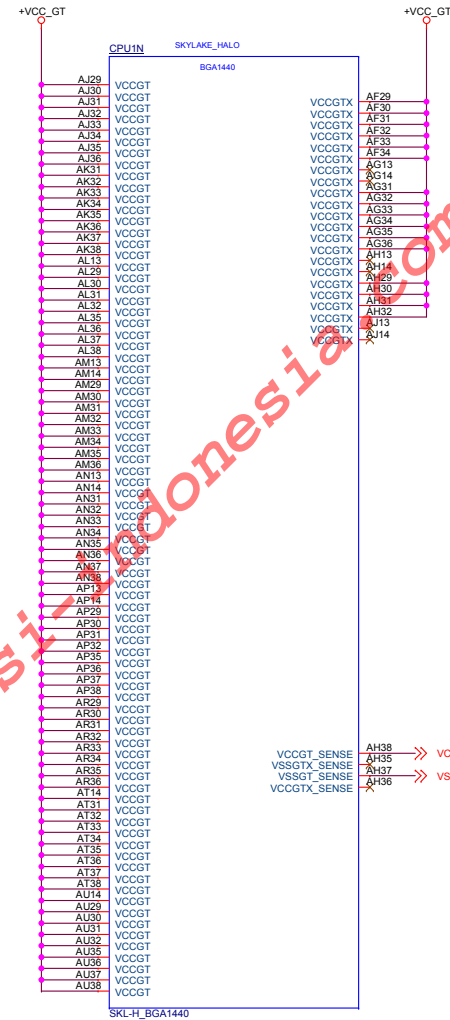
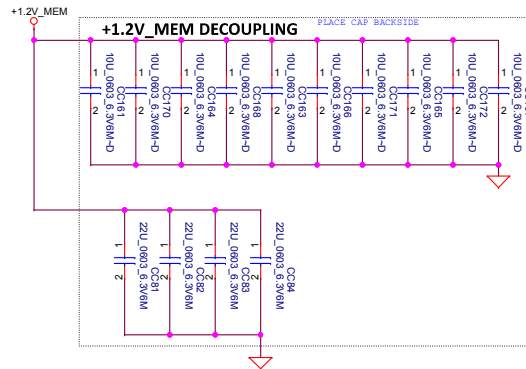
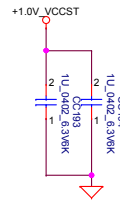
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For SKL-H 4+2
Remove VCCOPC/VCCEPIO/
VCCOPC_1P8 Cap



Remove VCC_SA cap
from EE side.



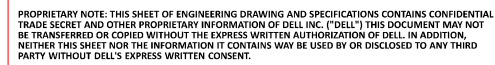
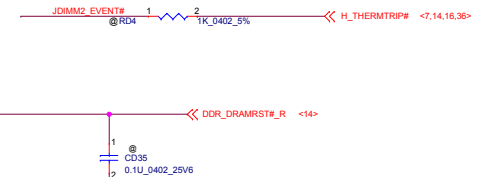
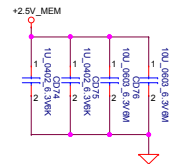
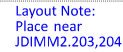
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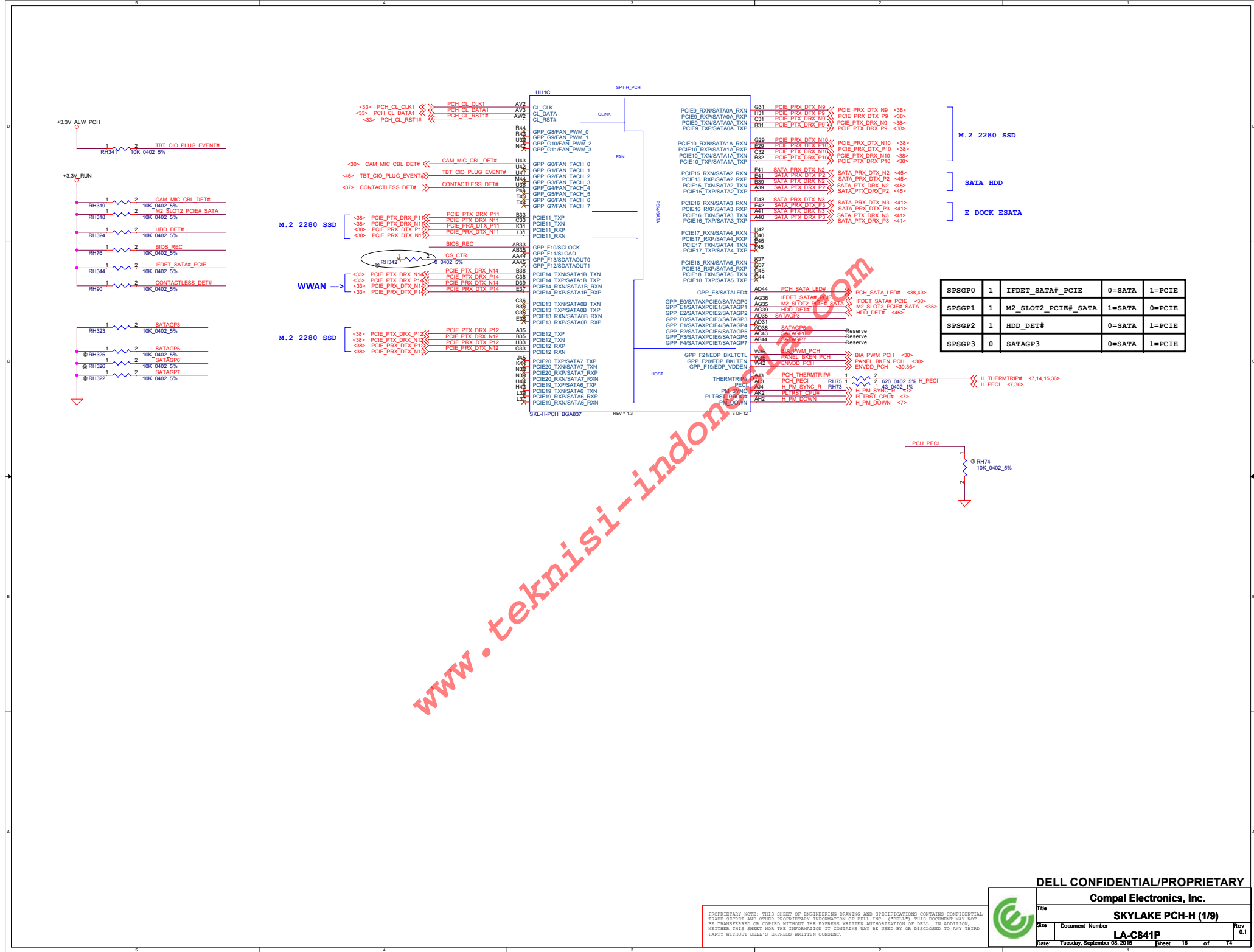
Compal Electronics, Inc.



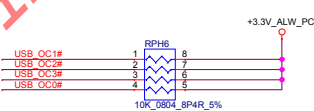
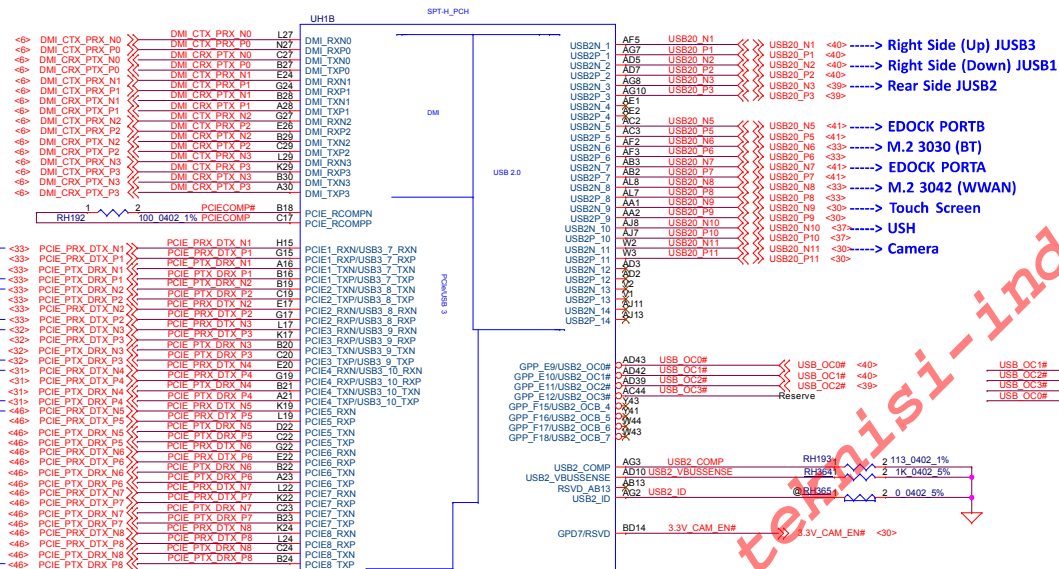
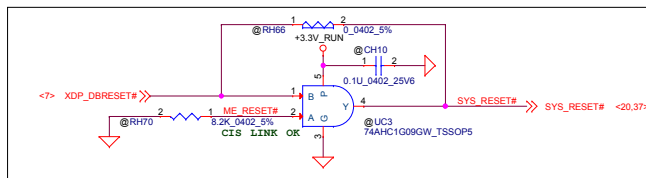
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Size	Document Number	LA-C841P	
Date	Tuesday, September 08, 2015	Sheet	12 of 74

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SPSPGP0	1	IFDET_SATA#_PCIE	0=SATA	1=PCIE
SPSPGP1	1	M2_SLOT2_PCIE#_SATA	1=SATA	0=PCIE
SPSPGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSPGP3	0	SATAGP3	0=SATA	1=PCIE



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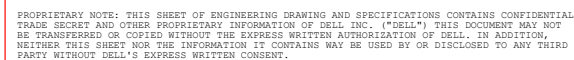
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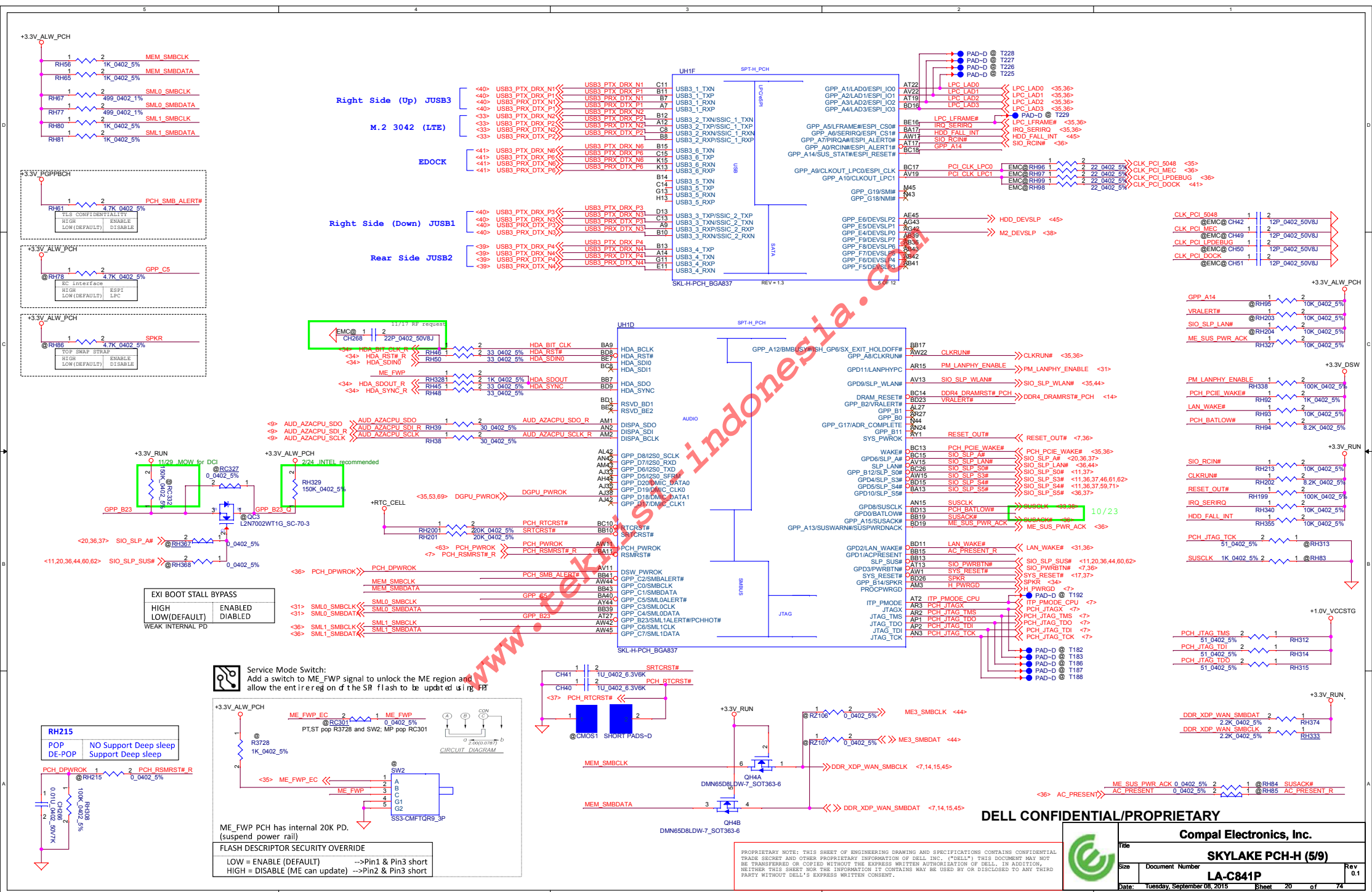
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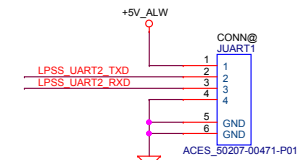
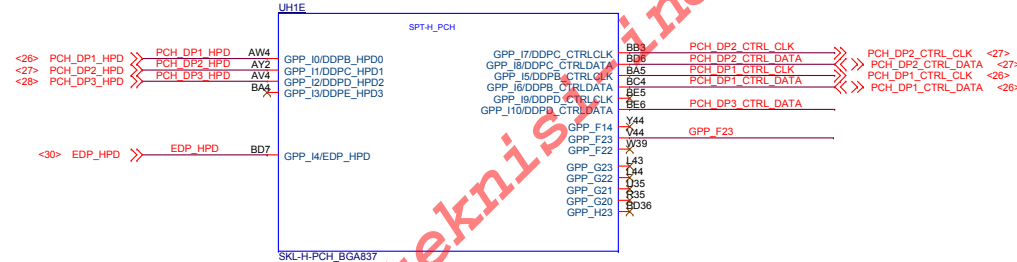
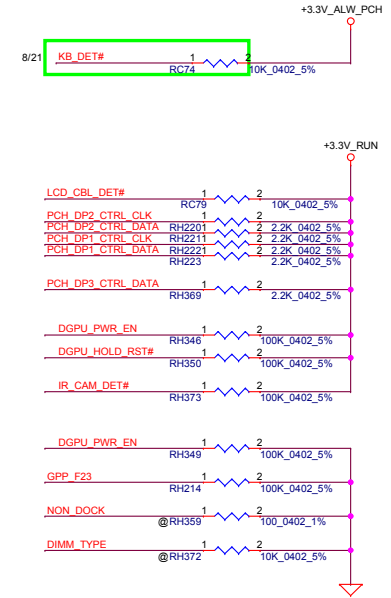
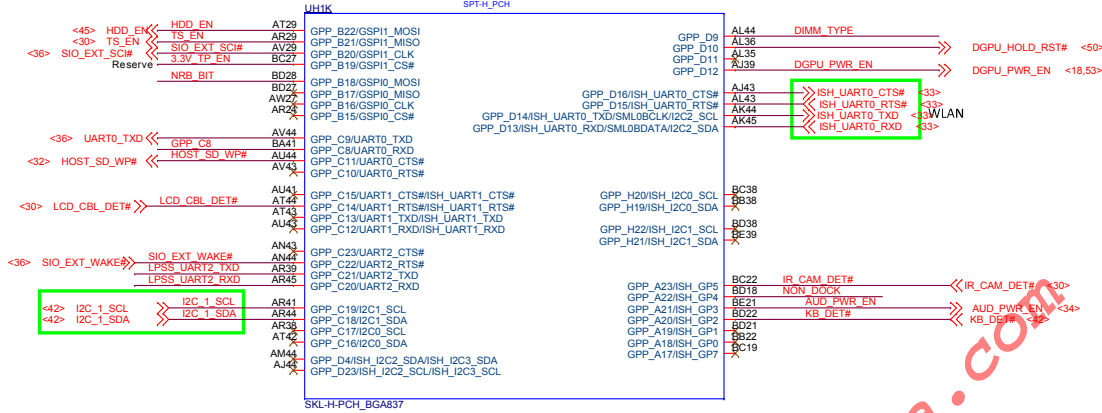
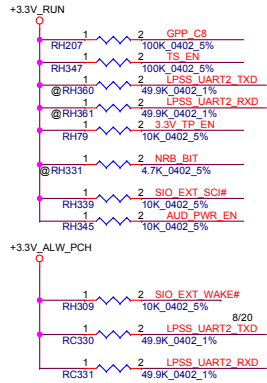
LA-C841P

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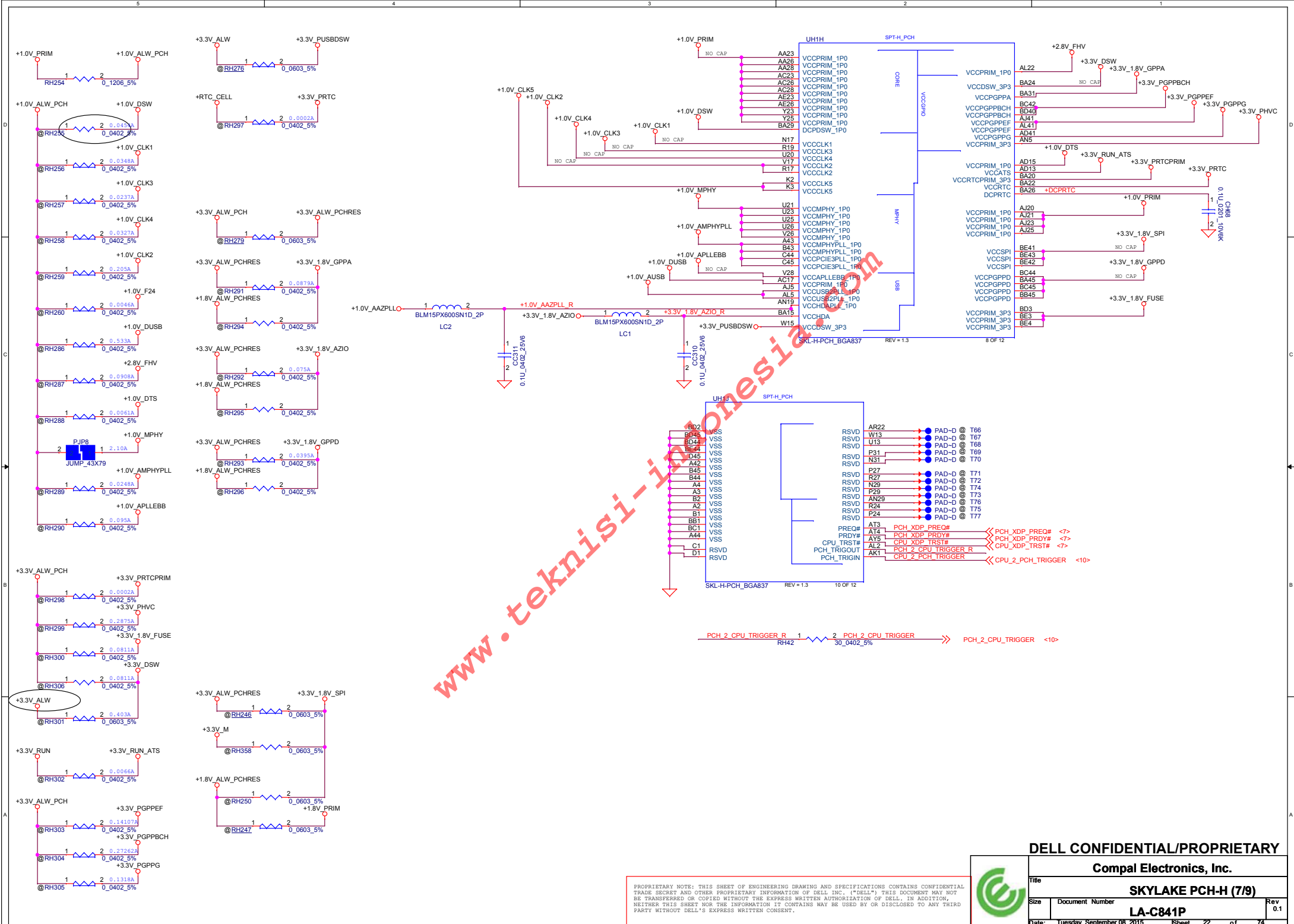
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Title	SKYLAKE PCH-H (6/9)		
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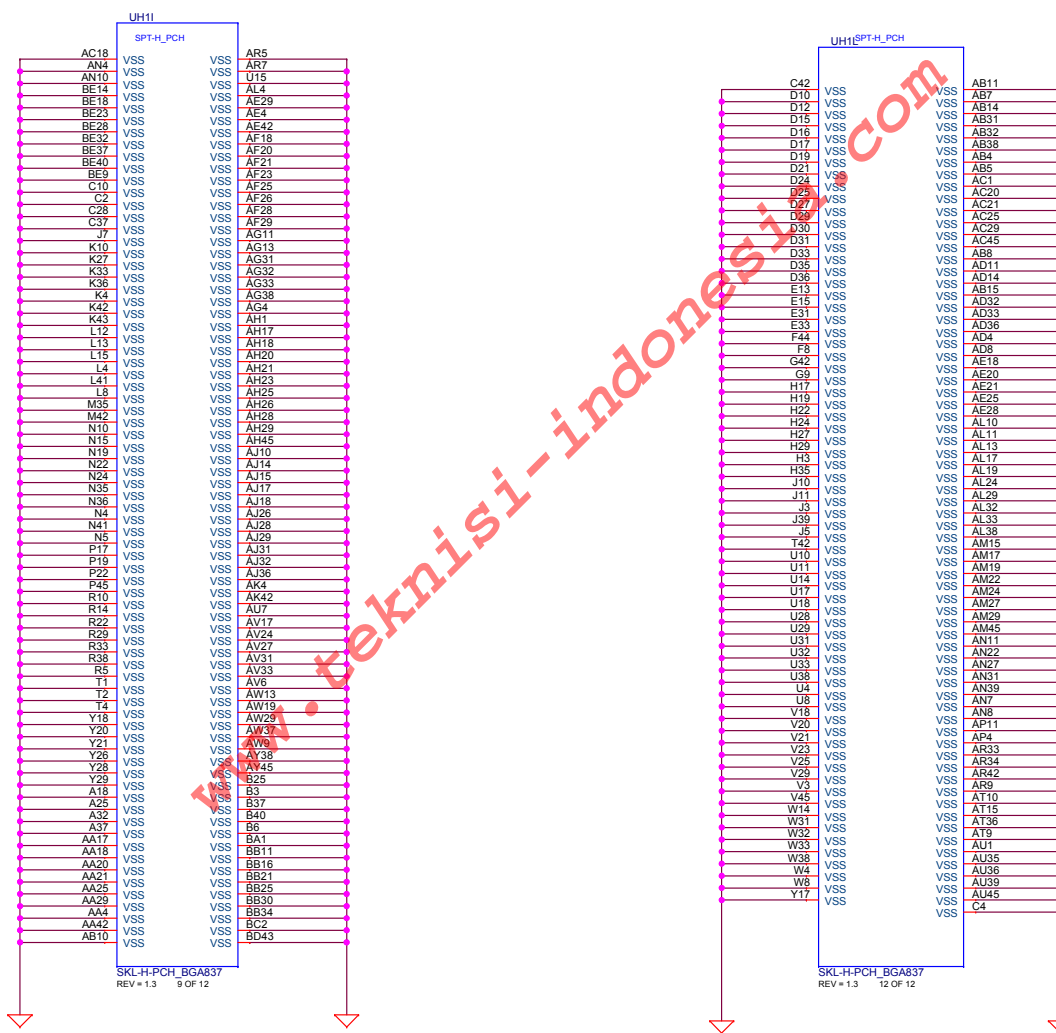
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Title			
SKYLAKE PCH-H (7/9)			
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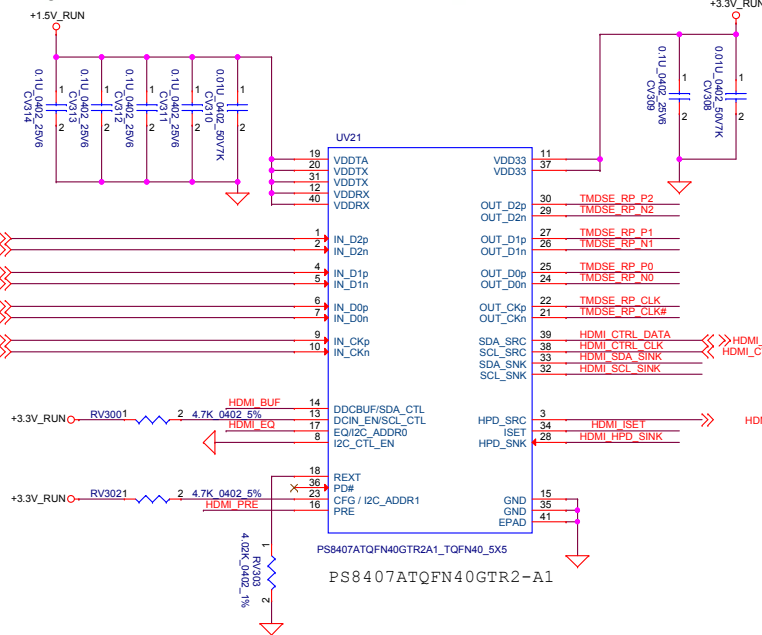
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Size Document Number LA-C841P Rev 0.1

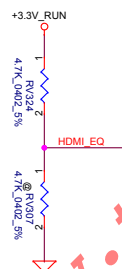
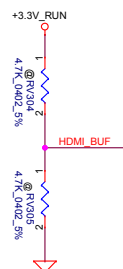
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D

<26> HDMI_TX_P2
<26> HDMI_TX_N2
<26> HDMI_TX_P1
<26> HDMI_TX_N1
<26> HDMI_TX_P0
<26> HDMI_TX_N0
<26> HDMI_CLKP
<26> HDMI_CLKN

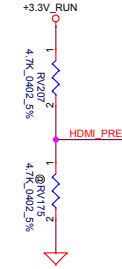
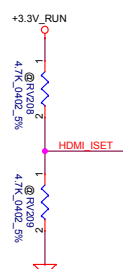


C



Enable active DDC buffer; Internal pull down at ~150kΩ, 3.3V
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC pass-through without internal pull up

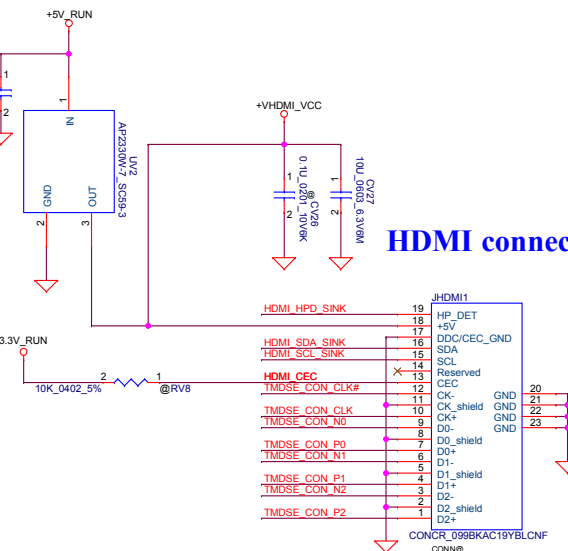
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB



TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V
L: default
H: increase +13%
M: reduce -13%

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

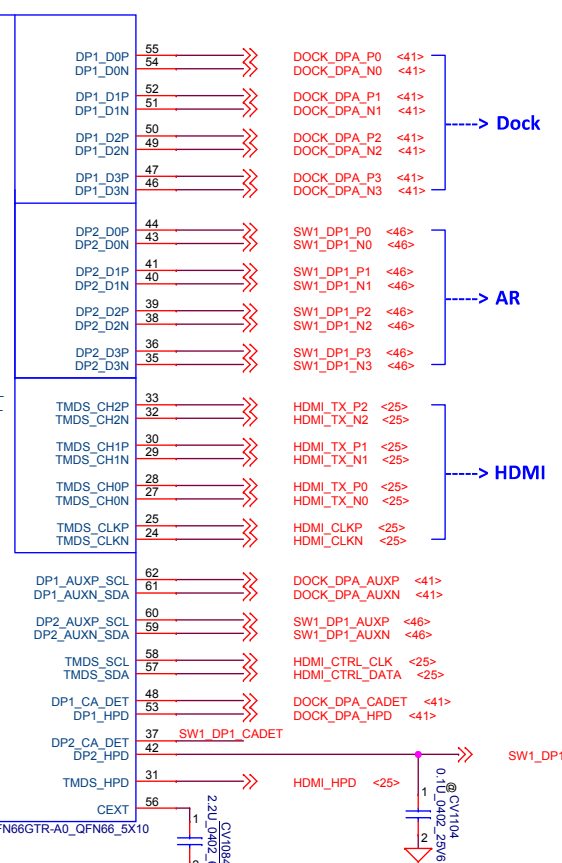
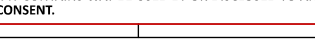
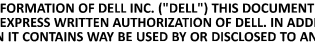
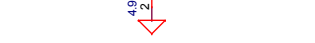
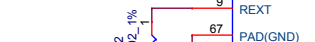
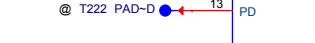
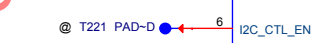
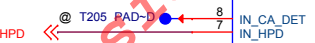
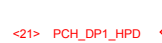
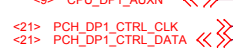
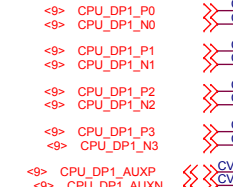
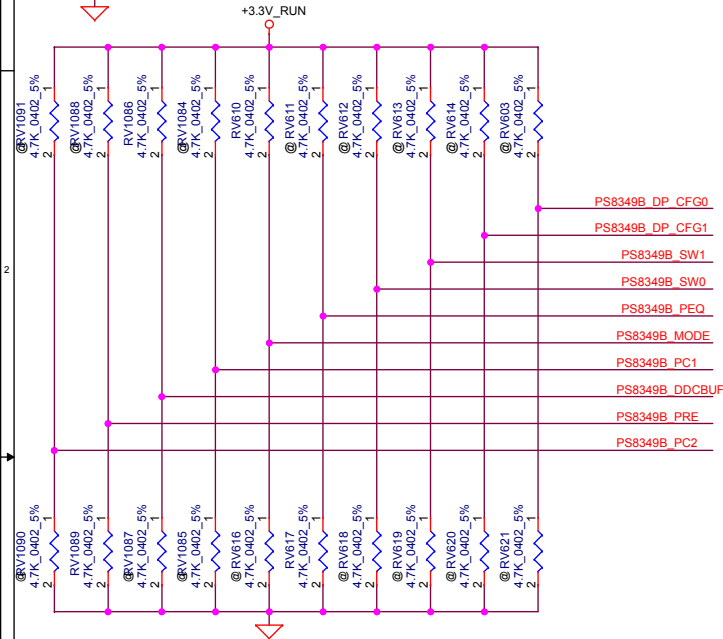
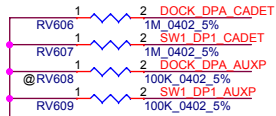
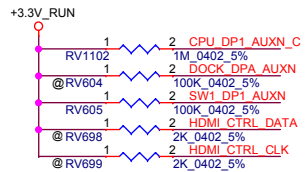
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HDMI connector

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Internally tied to VDD33/2 3.3V/I/O
PCx =
M:DP Portx output configuration is set by link training (default)
H:DP Portx output with fixed 800 mV and 0dB
L:DP Portx output with fixed 400 mV and 0dB
x=1, 2

Internally tied to VDD33/2 3.3V/I/O
TMDS PRE =
M:TMDS driver output with no pre-emphasis (default)
H:TMDS driver output with 2.4dB pre-emphasis
L:TMDS driver output with 3.3dB pre-emphasis

Internally pull down ~150K.3.3V I/O
For Control Switching (MODE = M), port is selected as follow:
[SW1,SW0] = [L,L], DP1 Port is selected (default)
[SW1,SW0] = [L,H], DP2 Port is selected
[SW1,SW0] = [H,L], TMDS Port is selected
[SW1,SW0] = [H,H], TMDS Port is selected
For Automatic Switching (MODE = H), port priority sequence is controlled as follow:
[SW1,SW0] = [L,L], DP1 Port > DP2 Port > TMDS Port (default)
[SW1,SW0] = [L,H], DP1 Port > TMDS Port > DP2 Port
[SW1,SW0] = [H,L], TMDS Port > DP2 Port > DP1 Port
[SW1,SW0] = [H,H], TMDS Port > DP1 Port > DP2 Port
[SW1,SW0] = [L,M], DP2 Port > DP1 Port > TMDS Port
[SW1,SW0] = [M,M], DP2 Port > TMDS Port > DP1 Port

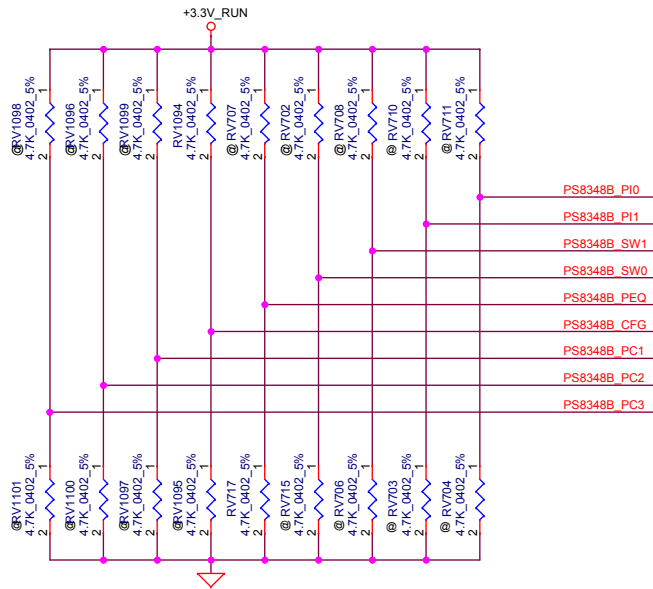
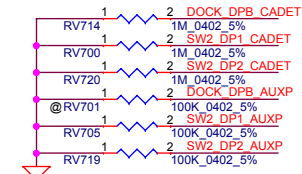
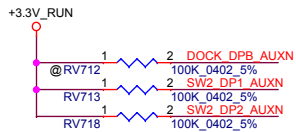
Internally tied to VDD33/2 3.3V/I/O
PEQ =
M:default, LEQ, compensate channel loss up to 12dB @ HBR2 (default)
H:HEQ, compensate channel loss up to 15dB @ HBR2
L:LLEQ, compensate channel loss up to 5dB @ HBR2

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Title			DP SW PS8349B		
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CPU_DP2_P0
 CPU_DP2_N0
 CPU_DP2_P1
 CPU_DP2_N1
 CPU_DP2_P2
 CPU_DP2_N2
 CPU_DP2_P3
 CPU_DP2_N3
 CPU_DP2_AUXP
 CPU_DP2_AUXN

CV1101 1 2 0.1u 0.402 25V6 CPU_DP2_P0_C 11
 CV1098 1 2 0.1u 0.402 25V6 CPU_DP2_N0_C 12
 CV1099 1 2 0.1u 0.402 25V6 CPU_DP2_P1_C 14
 CV1102 1 2 0.1u 0.402 25V6 CPU_DP2_N1_C 15
 CV1096 1 2 0.1u 0.402 25V6 CPU_DP2_P2_C 16
 CV1095 1 2 0.1u 0.402 25V6 CPU_DP2_N2_C 17
 CV1100 1 2 0.1u 0.402 25V6 CPU_DP2_P3_C 19
 CV1097 1 2 0.1u 0.402 25V6 CPU_DP2_N3_C 20
 CV1083 1 2 0.1u 0.402 25V6 CPU_DP2_AUXP_C 63
 CV1082 1 2 0.1u 0.402 25V6 CPU_DP2_AUXN_C 63

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<21> PCH_DP2_HPD

PS8348B PI0
 PS8348B PI1
 PS8348B SW1
 PS8348B SW0

PS8348B CFG
 PS8348B PC1
 PS8348B PC2
 PS8348B PC3

PS8348B PEQ
 PS8348B PD

PS8348B SW1
 PS8348B SW2

PS8348B SW1
 PS8348B SW2

PS8348B SW1
 PS8348B SW2

PS8348B SW1
 PS8348B SW2

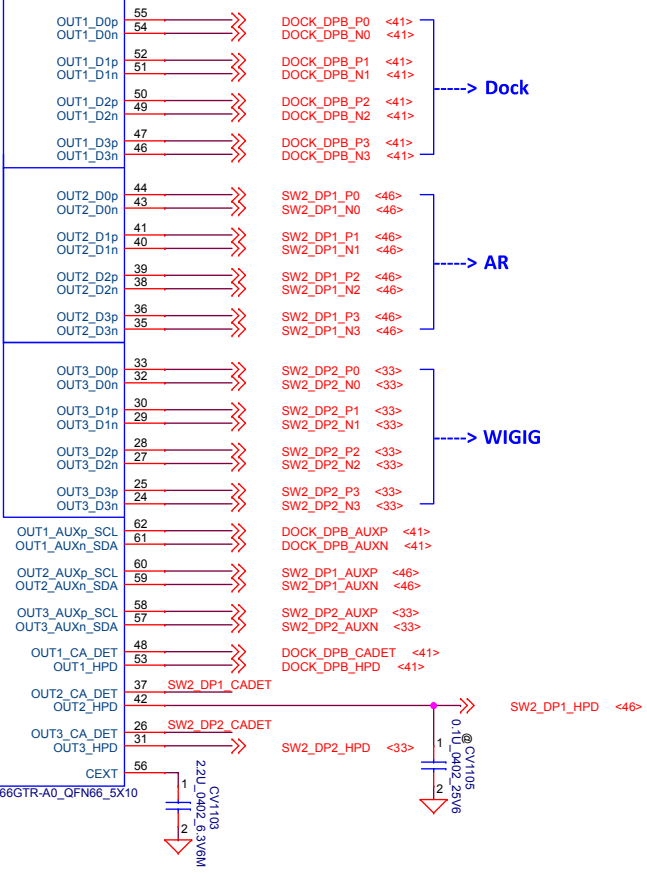
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PS8348B SW1
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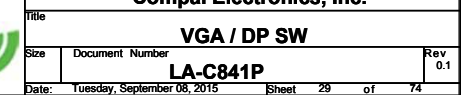
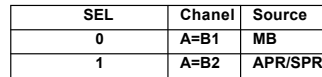
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 PS8348B SW2

PS8348B SW1
 PS8348B SW2

PS8348B SW1
 PS8348B SW2

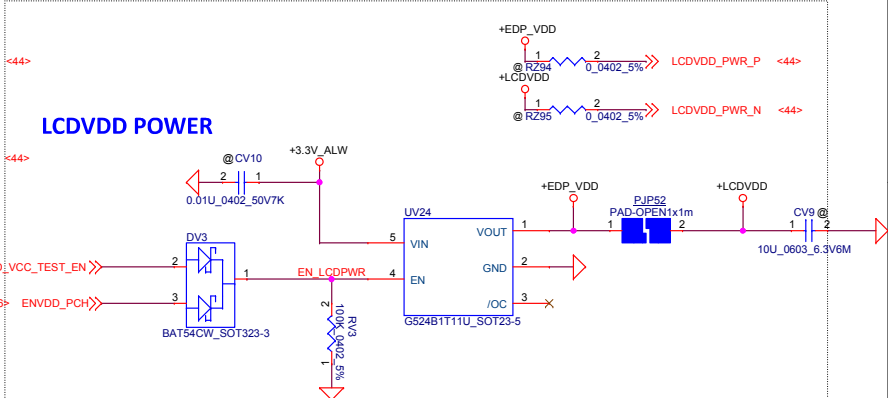
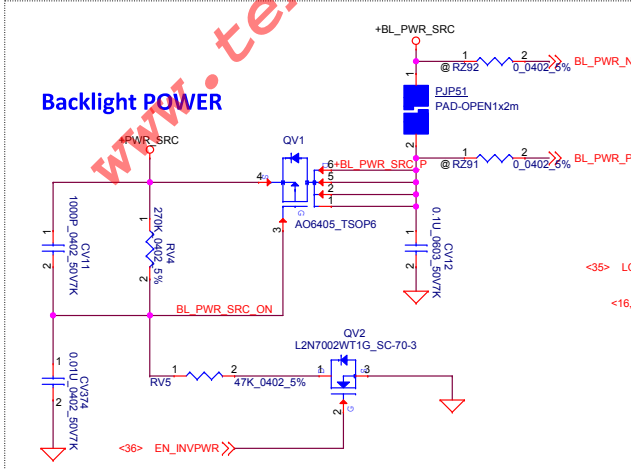
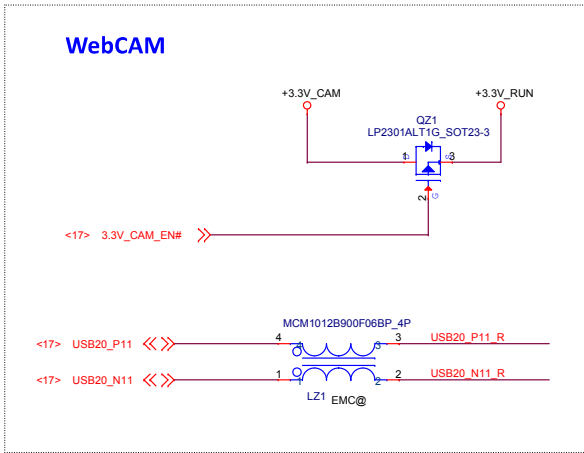
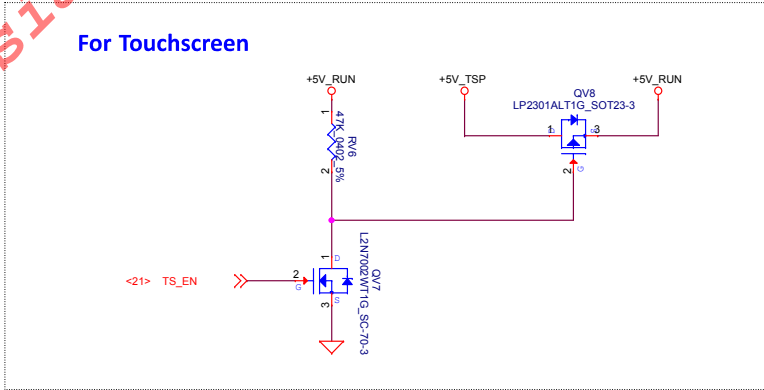
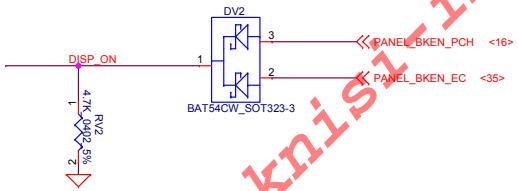
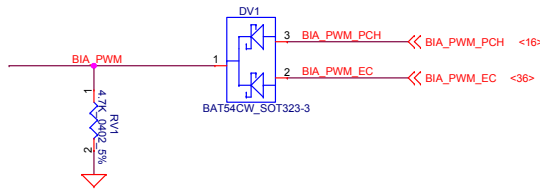
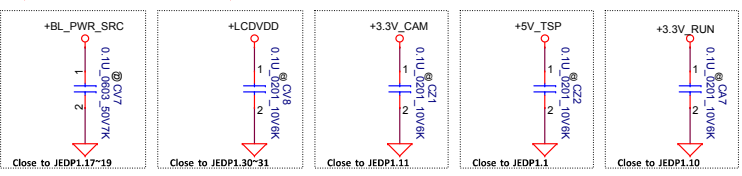
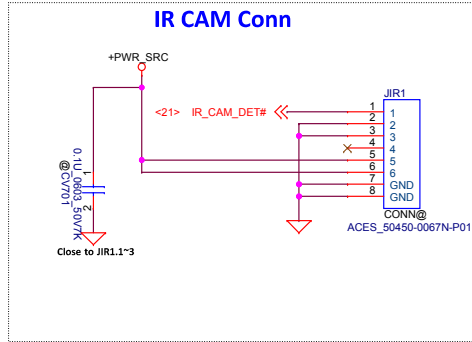
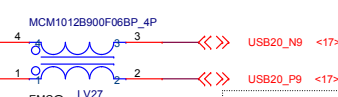
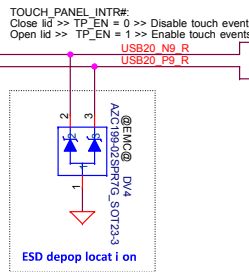
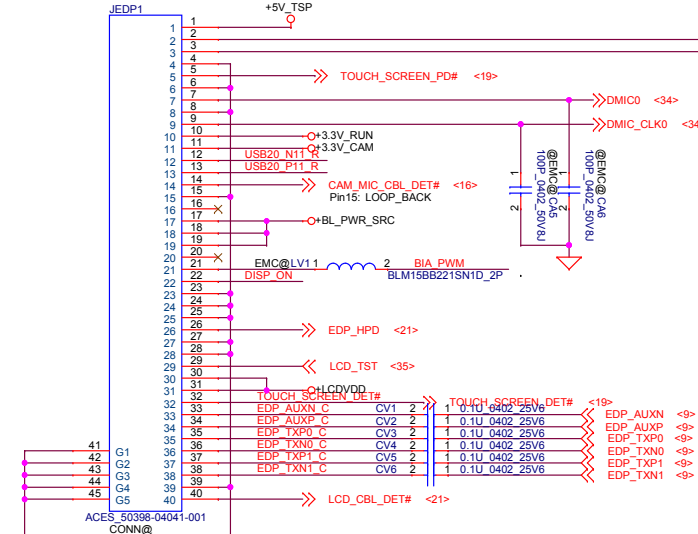


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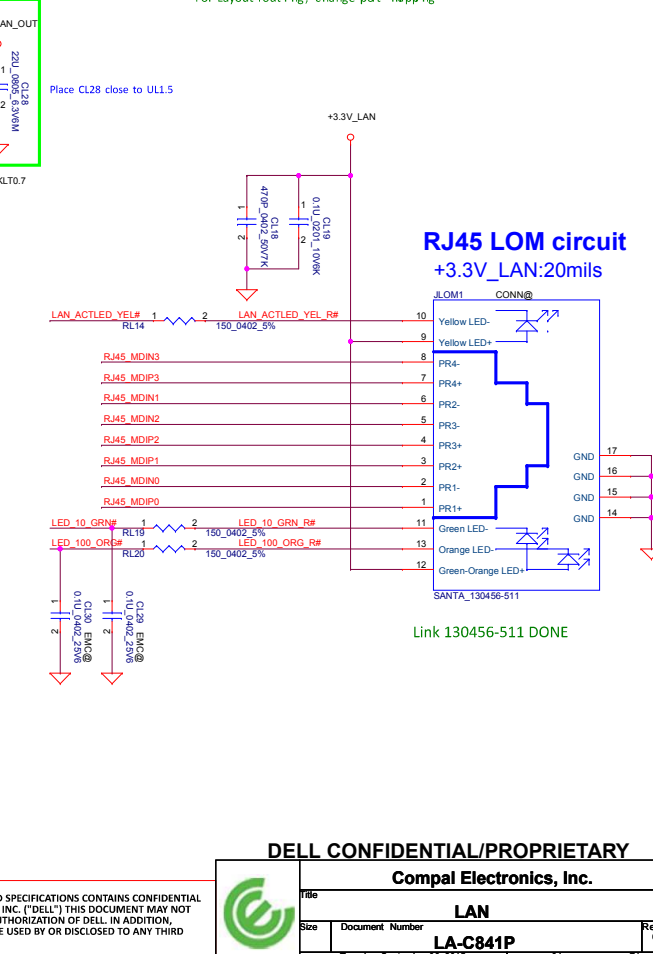
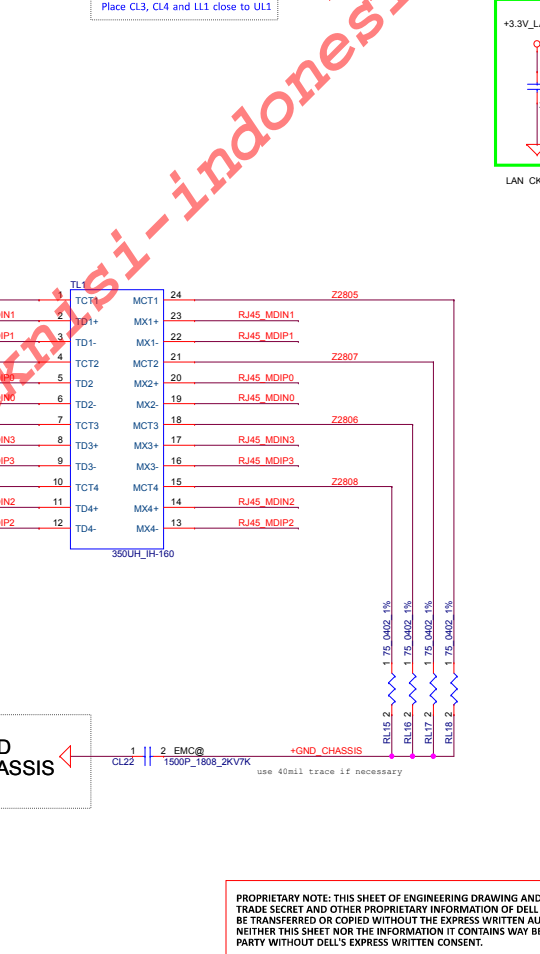
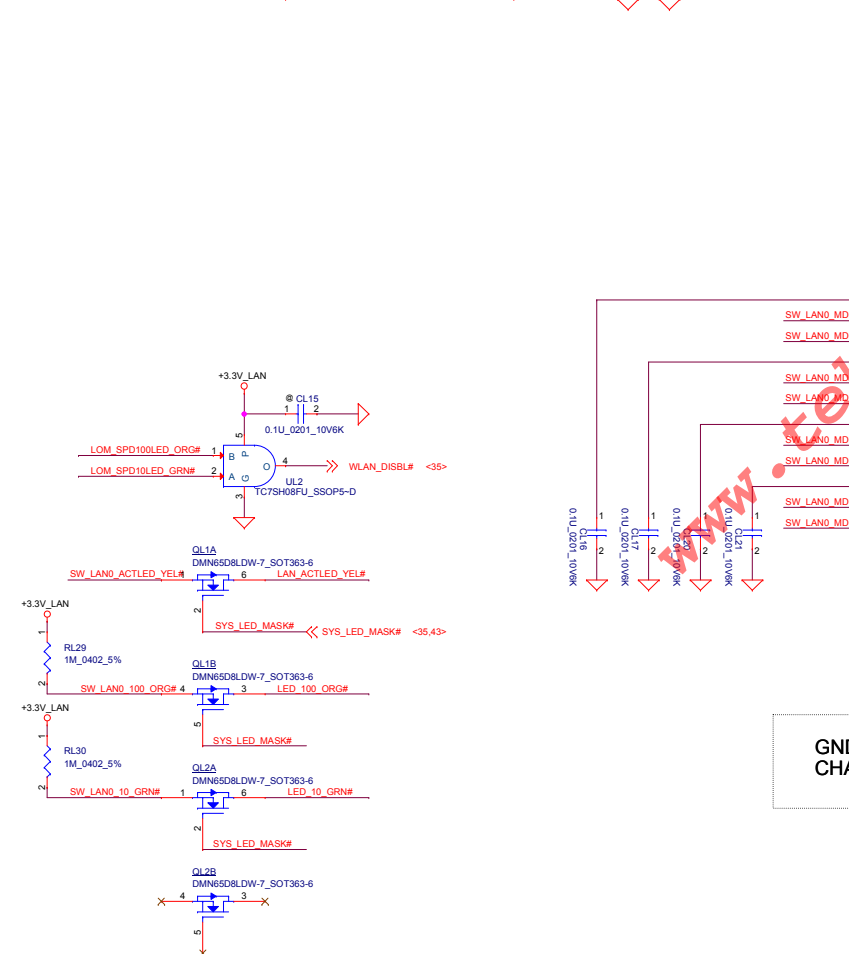
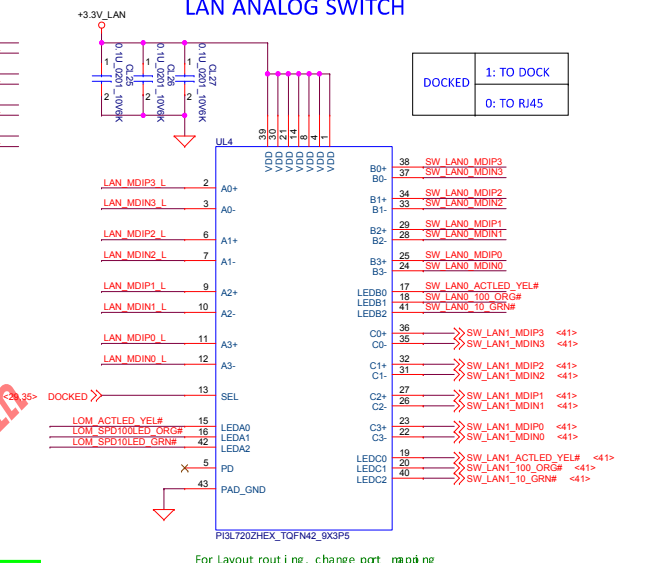
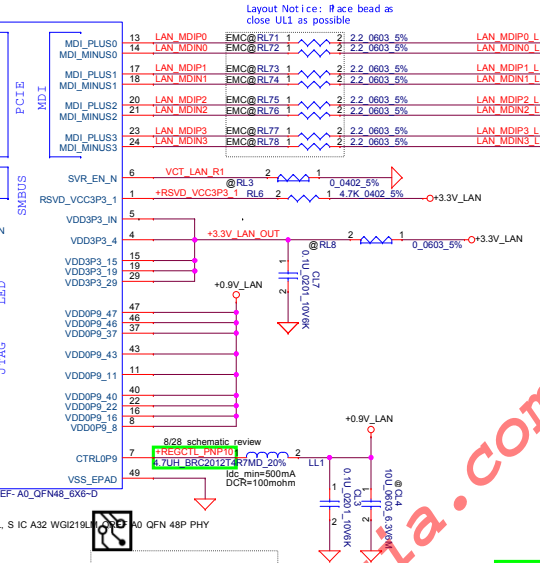
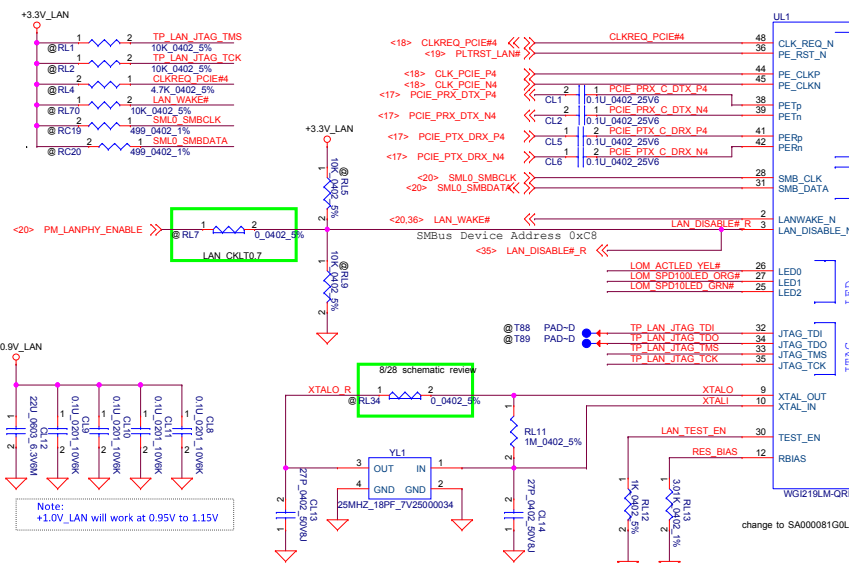


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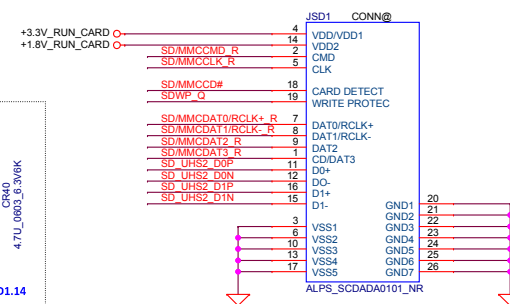
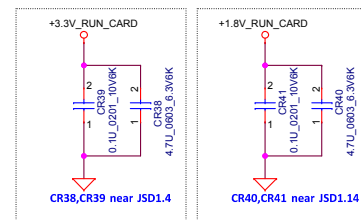
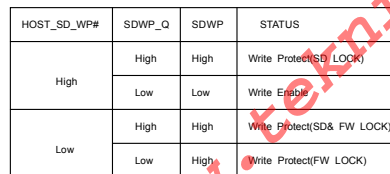


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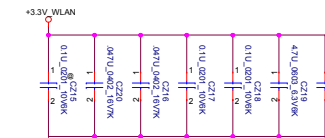
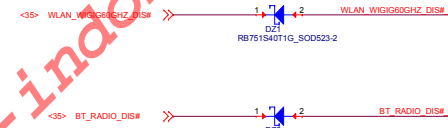
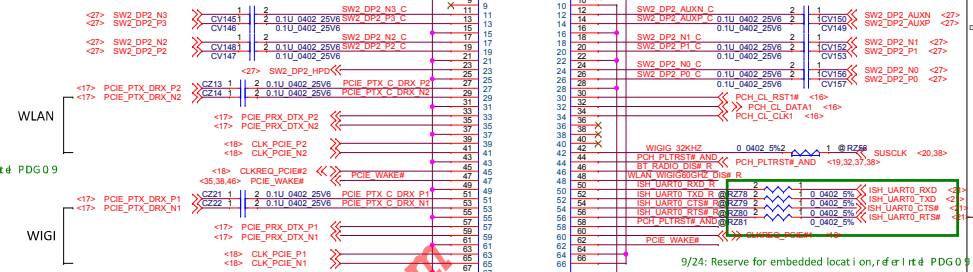
7/18 Vender suggest.



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NGFF slot A Key A
80148-3221&80148-4221 Footprint the same

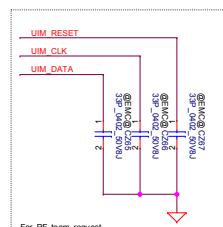


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

The schematic diagram shows the JSM1 module with the following connections:

- SIM_PWR** is connected to pin 1 (VCC).
- UIM_RESET** is connected to pin 2 (RST).
- UIM_CLK** is connected to pin 3 (CLK).
- UIM_DATA** is connected to pin 5 (VPP).
- RFU1** is connected to pin 7 (RFU2).
- DTSW** is connected to pin 9 (DTSW).
- GND** is connected to pins 10, 11, 12, 13, 14, and 15.
- R31** is a resistor connected to pin 16 (SIM_DET_B.1).
- SIM_DET_B.1** is a signal trace connected to pin 16.

The diagram also shows a signal trace for **SIM_DET_B.1** with a value of 0.0402_5M.



The diagram illustrates the electrical connections for a USB 3.0 to SATA bridge. Key components and signals include:

- USB 3.0 Connector (X1):** Signals include SIM_DET, CLK_PCE_P1, CLK_PCE_N1, and various data lines (D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100, D101, D102, D103, D104, D105, D106, D107, D108, D109, D110, D111, D112, D113, D114, D115, D116, D117, D118, D119, D120, D121, D122, D123, D124, D125, D126, D127, D128, D129, D130, D131, D132, D133, D134, D135, D136, D137, D138, D139, D140, D141, D142, D143, D144, D145, D146, D147, D148, D149, D150, D151, D152, D153, D154, D155, D156, D157, D158, D159, D160, D161, D162, D163, D164, D165, D166, D167, D168, D169, D170, D171, D172, D173, D174, D175, D176, D177, D178, D179, D180, D181, D182, D183, D184, D185, D186, D187, D188, D189, D190, D191, D192, D193, D194, D195, D196, D197, D198, D199, D200, D201, D202, D203, D204, D205, D206, D207, D208, D209, D210, D211, D212, D213, D214, D215, D216, D217, D218, D219, D220, D221, D222, D223, D224, D225, D226, D227, D228, D229, D230, D231, D232, D233, D234, D235, D236, D237, D238, D239, D240, D241, D242, D243, D244, D245, D246, D247, D248, D249, D250, D251, D252, D253, D254, D255, D256, D257, D258, D259, D260, D261, D262, D263, D264, D265, D266, D267, D268, D269, D270, D271, D272, D273, D274, D275, D276, D277, D278, D279, D280, D281, D282, D283, D284, D285, D286, D287, D288, D289, D290, D291, D292, D293, D294, D295, D296, D297, D298, D299, D300, D301, D302, D303, D304, D305, D306, D307, D308, D309, D310, D311, D312, D313, D314, D315, D316, D317, D318, D319, D320, D321, D322, D323, D324, D325, D326, D327, D328, D329, D330, D331, D332, D333, D334, D335, D336, D337, D338, D339, D340, D341, D342, D343, D344, D345, D346, D347, D348, D349, D350, D351, D352, D353, D354, D355, D356, D357, D358, D359, D360, D361, D362, D363, D364, D365, D366, D367, D368, D369, D370, D371, D372, D373, D374, D375, D376, D377, D378, D379, D380, D381, D382, D383, D384, D385, D386, D387, D388, D389, D390, D391, D392, D393, D394, D395, D396, D397, D398, D399, D400, D401, D402, D403, D404, D405, D406, D407, D408, D409, D410, D411, D412, D413, D414, D415, D416, D417, D418, D419, D420, D421, D422, D423, D424, D425, D426, D427, D428, D429, D430, D431, D432, D433, D434, D435, D436, D437, D438, D439, D440, D441, D442, D443, D444, D445, D446, D447, D448, D449, D450, D451, D452, D453, D454, D455, D456, D457, D458, D459, D460, D461, D462, D463, D464, D465, D466, D467, D468, D469, D470, D471, D472, D473, D474, D475, D476, D477, D478, D479, D480, D481, D482, D483, D484, D485, D486, D487, D488, D489, D490, D491, D492, D493, D494, D495, D496, D497, D498, D499, D500, D501, D502, D503, D504, D505, D506, D507, D508, D509, D510, D511, D512, D513, D514, D515, D516, D517, D518, D519, D520, D521, D522, D523, D524, D525, D526, D527, D528, D529, D530, D531, D532, D533, D534, D535, D536, D537, D538, D539, D540, D541, D542, D543, D544, D545, D546, D547, D548, D549, D550, D551, D552, D553, D554, D555, D556, D557, D558, D559, D560, D561, D562, D563, D564, D565, D566, D567, D568, D569, D570, D571, D572, D573, D574, D575, D576, D577, D578, D579, D580, D581, D582, D583, D584, D585, D586, D587, D588, D589, D590, D591, D592, D593, D594, D595, D596, D597, D598, D599, D600, D601, D602, D603, D604, D605, D606, D607, D608, D609, D610, D611, D612, D613, D614, D615, D616, D617, D618, D619, D620, D621, D622, D623, D624, D625, D626, D627, D628, D629, D630, D631, D632, D633, D634, D635, D636, D637, D638, D639, D640, D641, D642, D643, D644, D645, D646, D647, D648, D649, D650, D651, D652, D653, D654, D655, D656, D657, D658, D659, D660, D661, D662, D663, D664, D665, D666, D667, D668, D669, D670, D671, D672, D673, D674, D675, D676, D677, D678, D679, D680, D681, D682, D683, D684, D685, D686, D687, D688, D689, D690, D691, D692, D693, D694, D695, D696, D697, D698, D699, D700, D701, D702, D703, D704, D705, D706, D707, D708, D709, D710, D711, D712, D713, D714, D715, D716, D717, D718, D719, D720, D721, D722, D723, D724, D725, D726, D727, D728, D729, D730, D731, D732, D733, D734, D735, D736, D737, D738, D739, D740, D741, D742, D743, D744, D745, D746, D747, D748, D749, D750, D751, D752, D753, D754, D755, D756, D757, D758, D759, D760, D761, D762, D763, D764, D765, D766, D767, D768, D769, D770, D771, D772, D773, D774, D775, D776, D777, D778, D779, D780, D781, D782, D783, D784, D785, D786

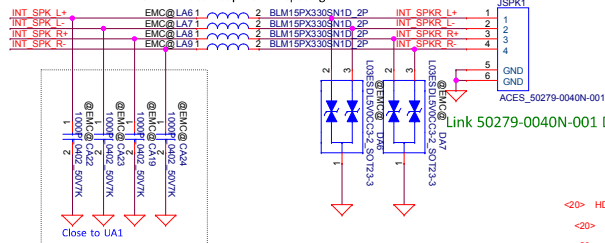
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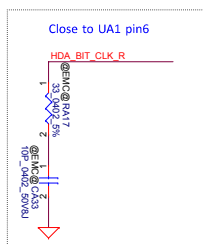
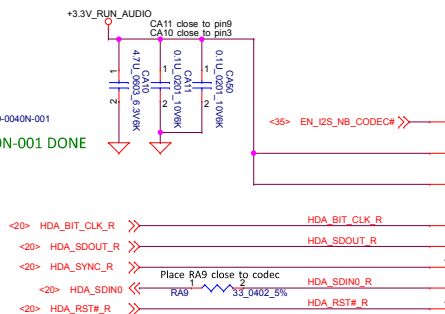
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Internal Speakers Header

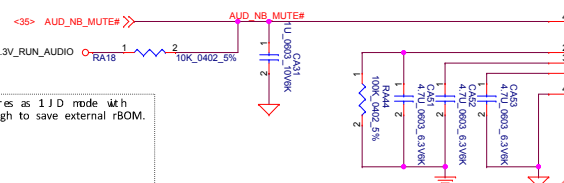
40 mils trace keep 20 mil spacing



Link 50279-0040N-001 DONE



BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

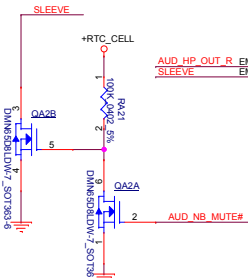


Verb table configures as 1JD mode with
internal 47K pull high to save external rBOM.

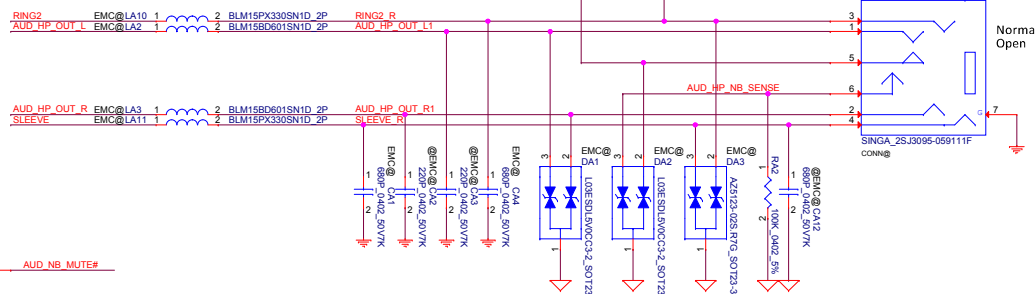
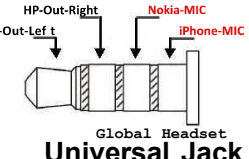
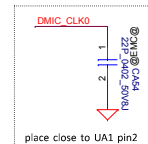
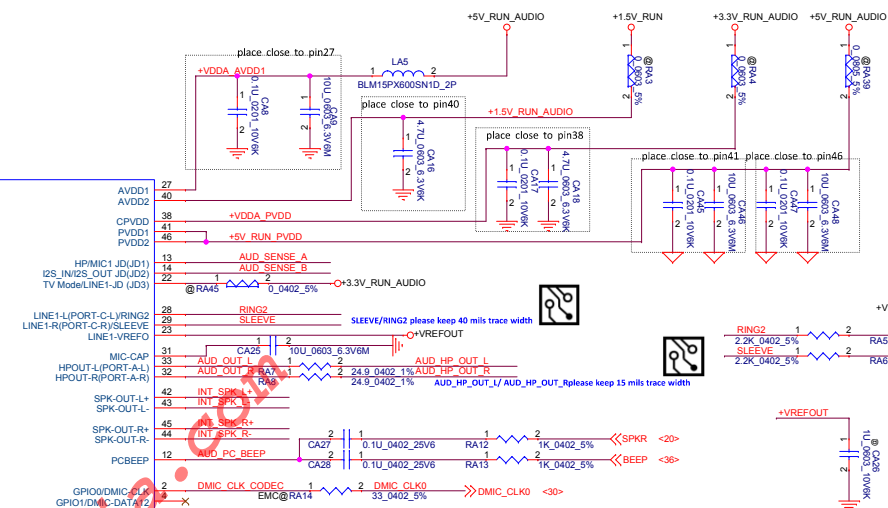
A circuit diagram showing the connection of the L297002V11C_SG-70-3 DAC to the AUD_HPB_NB_SENSE pin. The DAC's output (pin 1) is connected to the sense pin (pin 1) through a 20k resistor. The DAC's ground (pin 3) is connected to the common ground. The sense pin is also connected to the common ground through a 10k resistor. A note indicates that this configuration is added to solve pop noise and detect issues.

[illegible]

Power sequence +5V_BUN_AUDIO(501 μs) ≥ +3.3V_BUN_AUDIO(1204 μs) ≥ +1.5V_BUN



Realtek feedback
Prevent the Noise from Combo Jack
while system entry into S3 / S4 / S5



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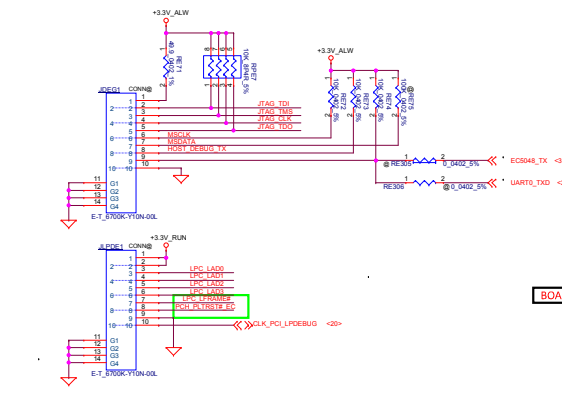
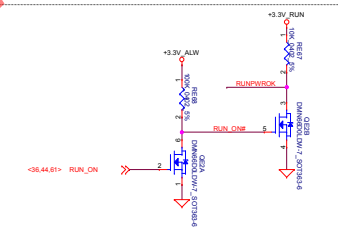
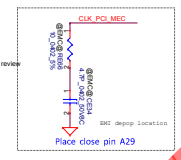
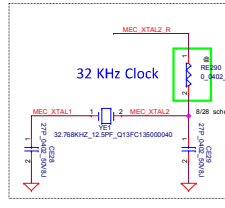
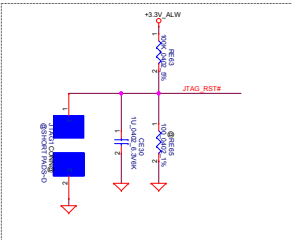
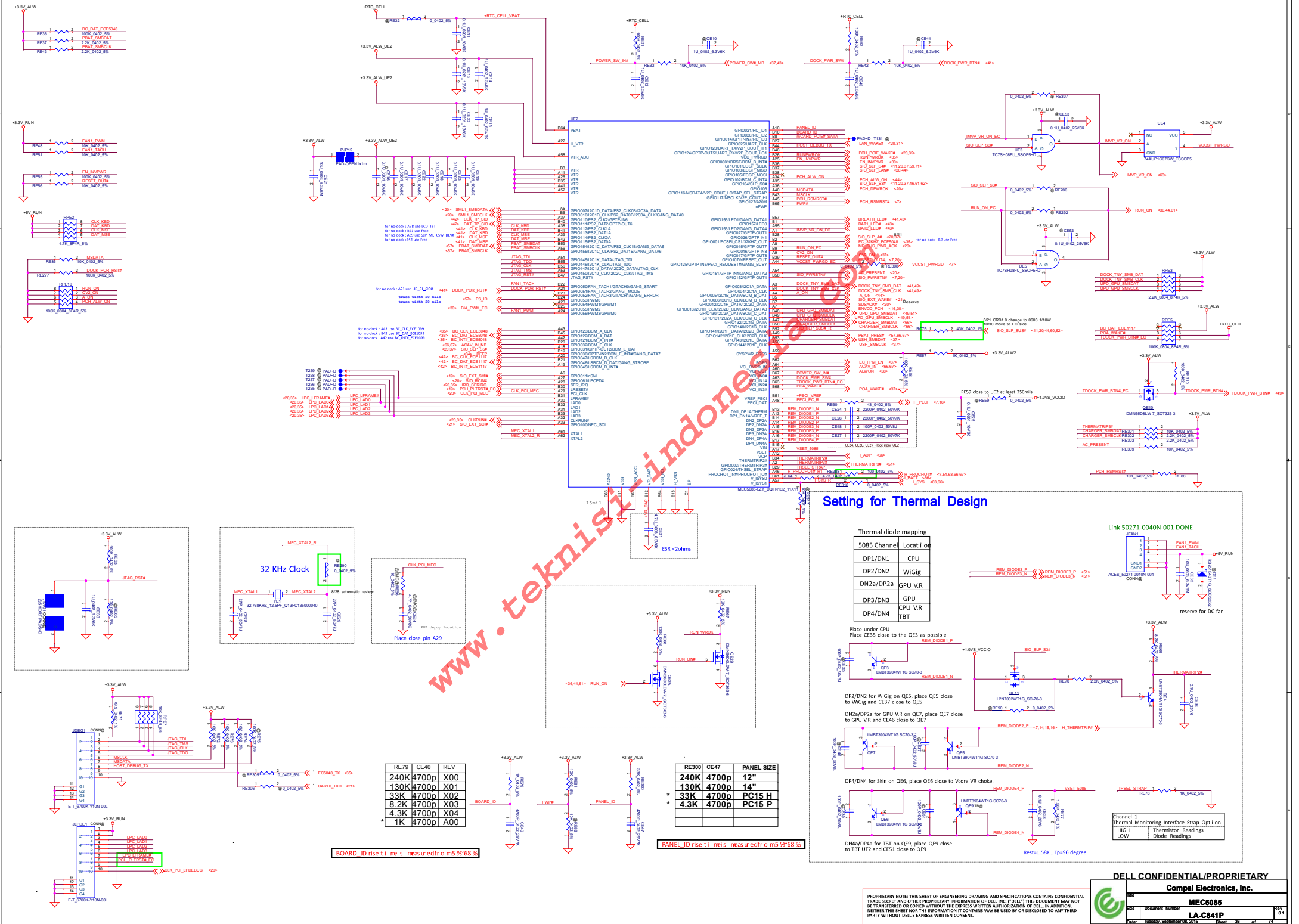
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Codec ALC3235

LA-C841B

Rev
0.

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RE79	CE40	REV
240K 4700p	X00	
130K 4700p	X01	
33K 4700p	X02	
8.2K 4700p	X03	
4.3K 4700p	X04	
1K 4700p	A00	

BOARD_ID rise t1 me1 meas ure d f o m S %68 %

RE300	CE47	PANEL SIZE
240K 4700p	12"	
130K 4700p	14"	
33K 4700p	PC15 H	
4.3K 4700p	PC15 P	

PANEL_ID rise t1 me1 meas ure d f o m S %68 %

Setting for Thermal Design

Thermal diode mapping	
DP1/DN1	CPU
DP2/DN2	WiGig
DN2a/DP2a	GPU V.R
DP3/DN3	GPU
DP4/DN4	CPU V.R
	TBT

Place under CPU

Place CE35 close to the QE3 as possible

WiGig and CE37 close to QE5

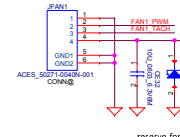
DN2a/DP2a for GPU V.R on QE7, place QE7 close to GPU V.R and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

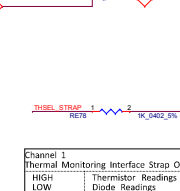
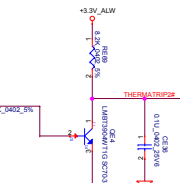
DN4a/DP4a for TBT on QE9, place QE9 close to TBT UT2 and CE51 close to QE9

Rest=1.58K, Tj=96 degree

Link 50271-0040N-001 DONE



reserve for DC fan



Channel 1 Thermal Monitoring Interface Strap Opt on HIGH LOW Thermistor Readings Diode Readings

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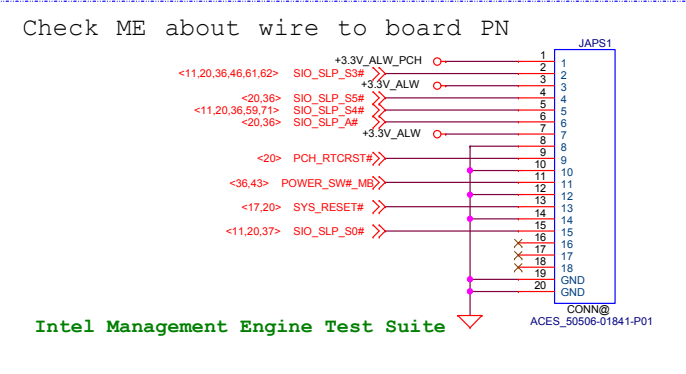
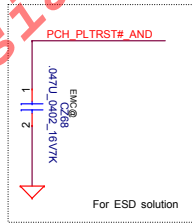
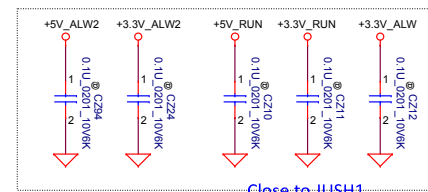
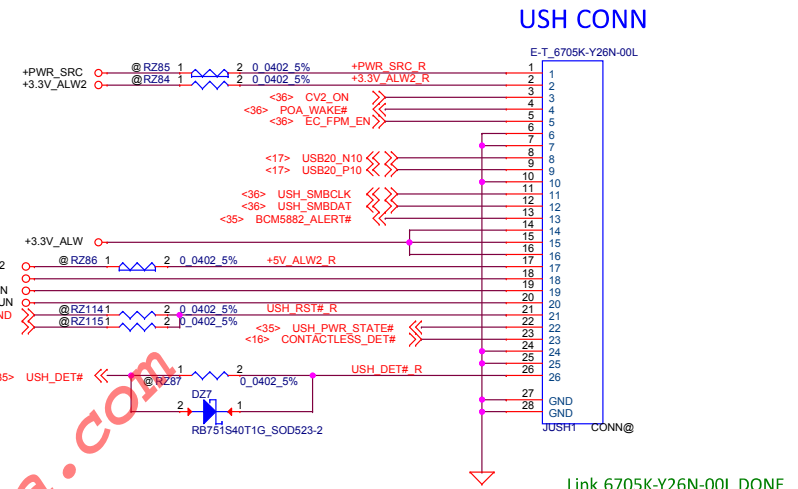
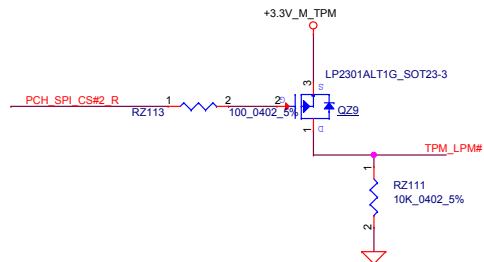
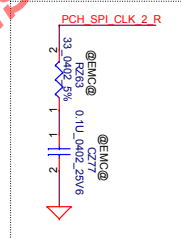
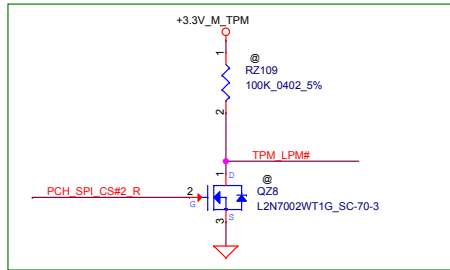
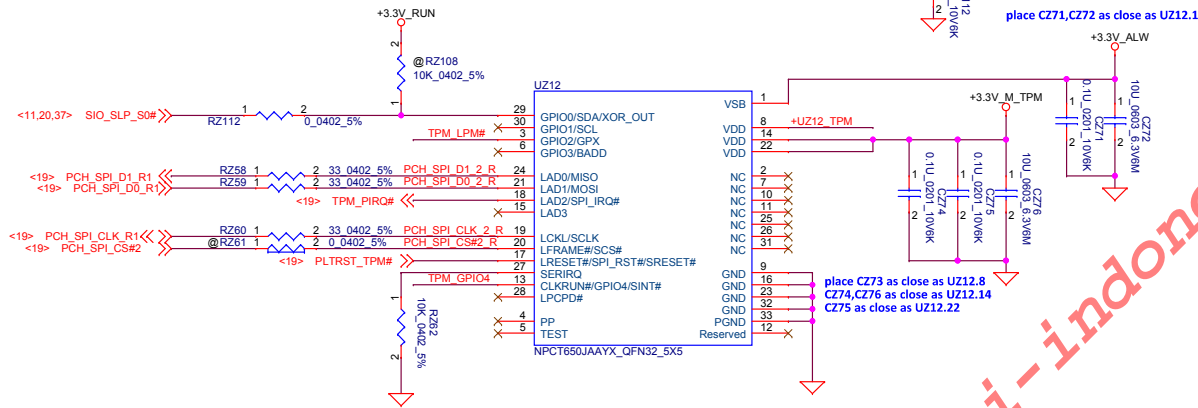
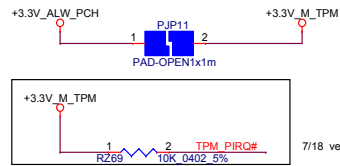
MEC5085

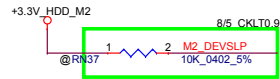
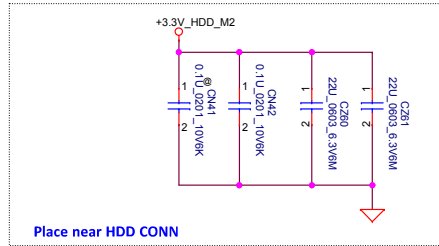
LA-C841P

Rev 0.1

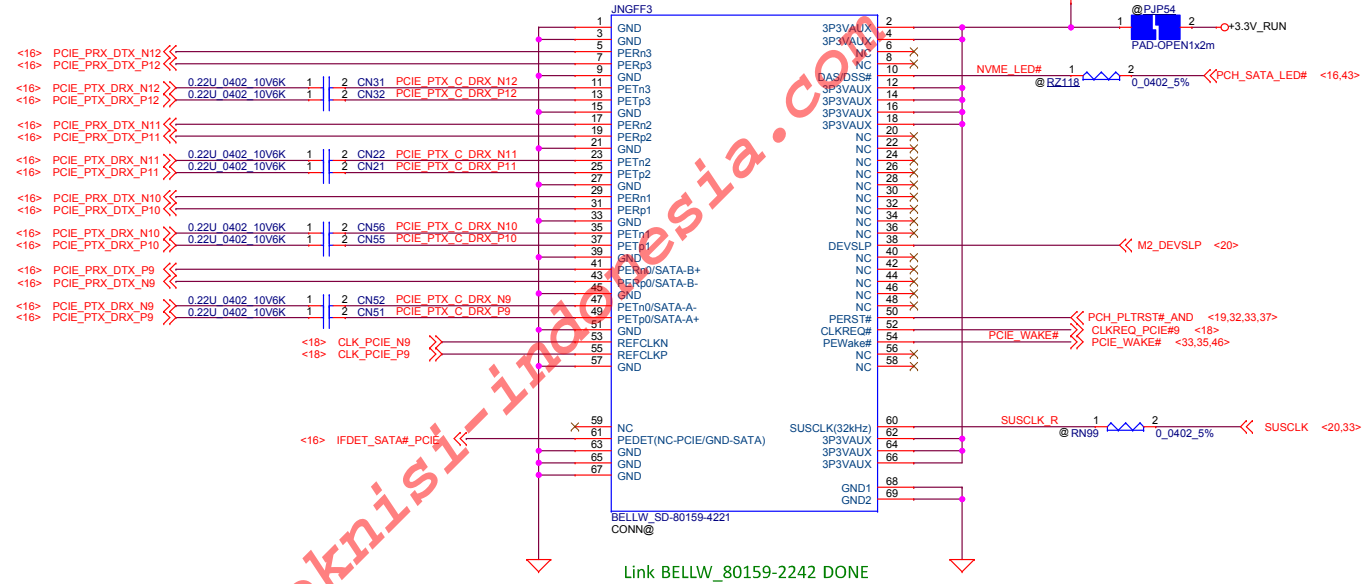
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The schematic shows a 5% tolerance resistor connected between the +3.3V_M and +3.3V_M-TPM pins. The resistor is labeled with the value 0 0603 5% and the component identifier @RZ72 1.





2280 SSD NGFF slot C Key M



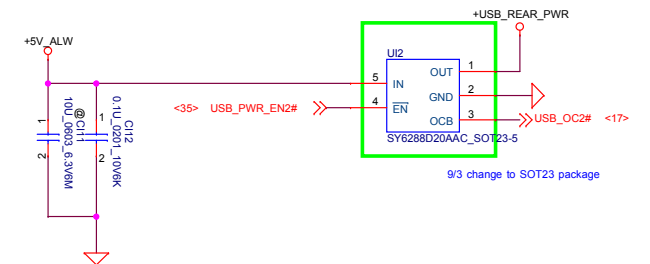
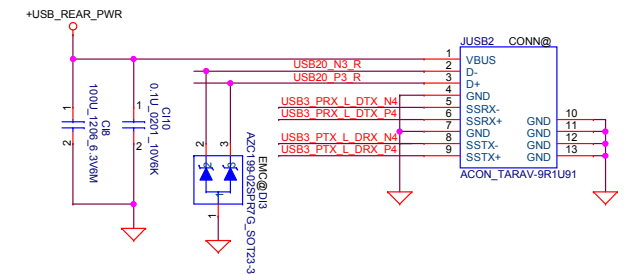
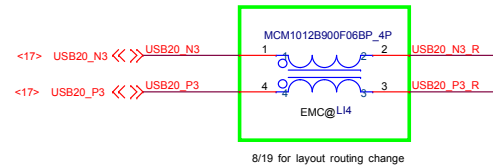
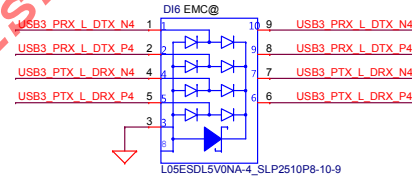
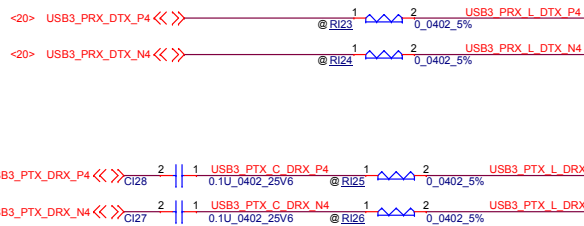
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Size	Document Number		Rev
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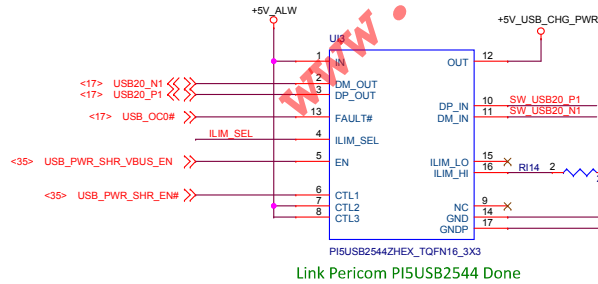
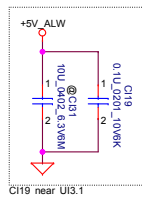
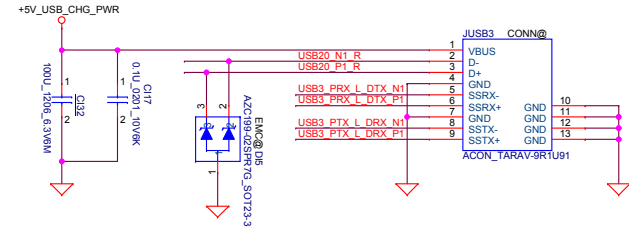
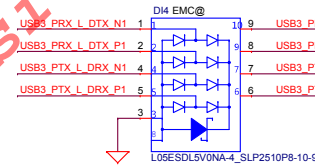
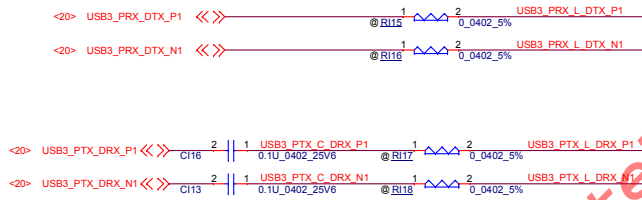
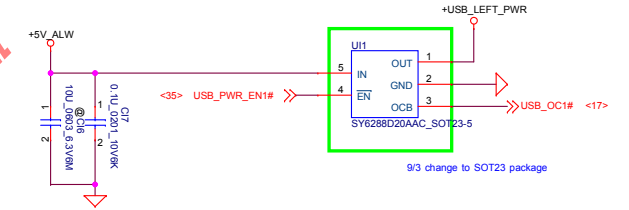
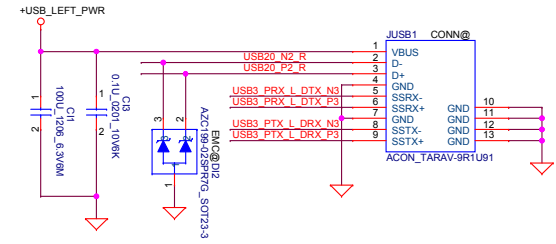
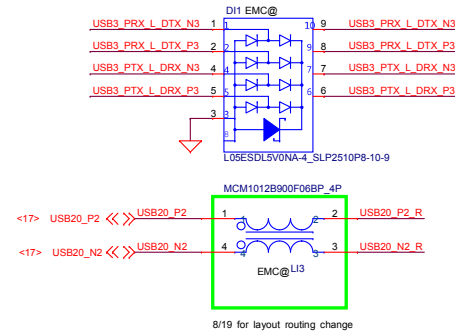
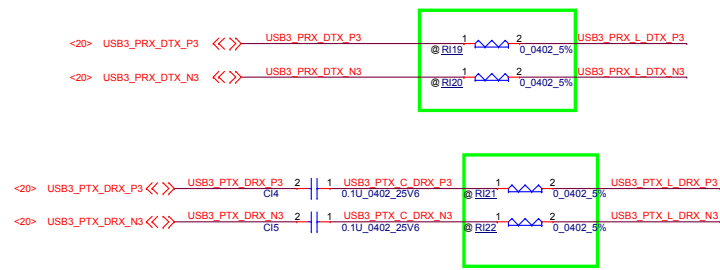
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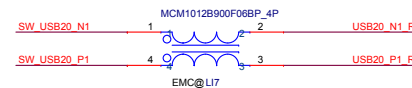
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Title		USB SW	
Size	Document Number	Rev	
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Date:	Tuesday, September 08, 2015	Sheet	39 of 74



Link Pericom PISUSB2544 Done



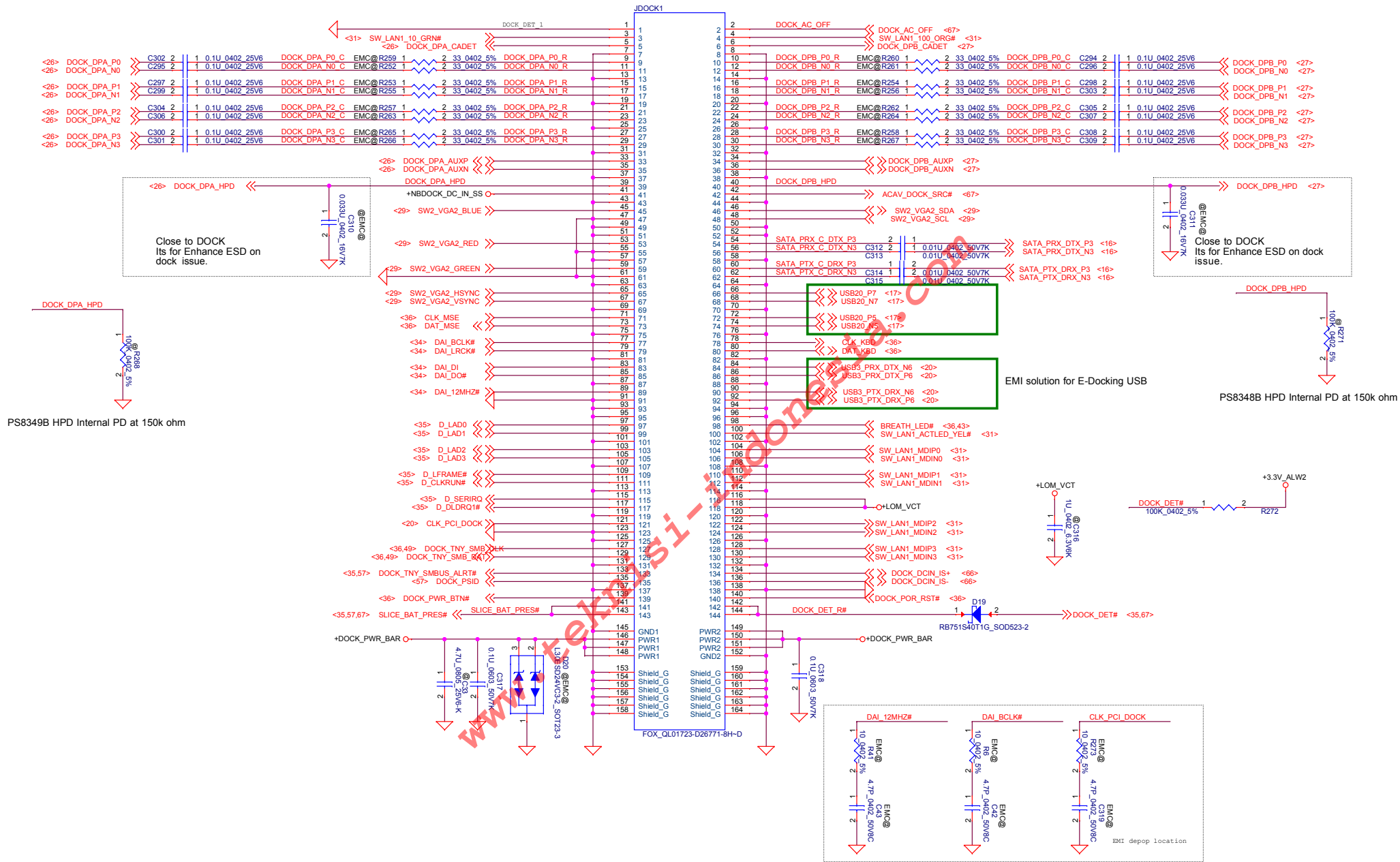
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Title		USB3.0
Size	Document Number	LA-C841P
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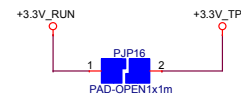
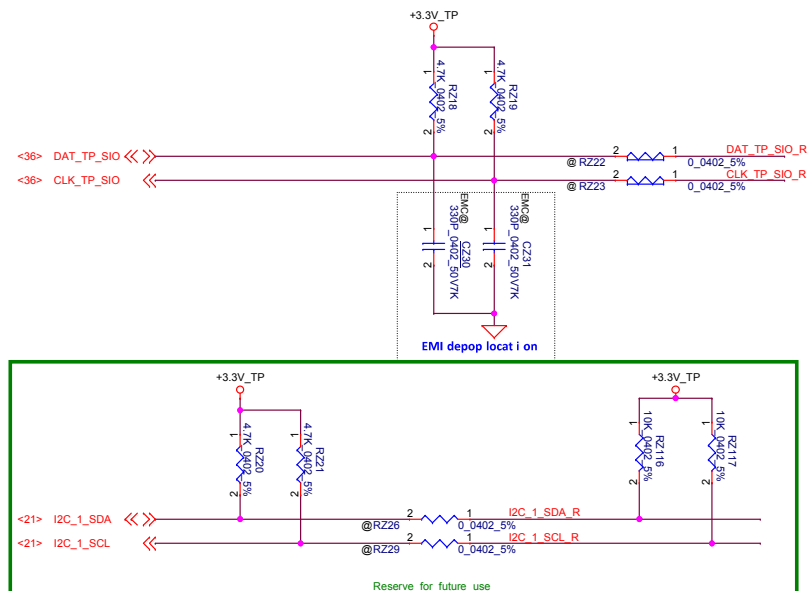
Compal Electronics, Inc.



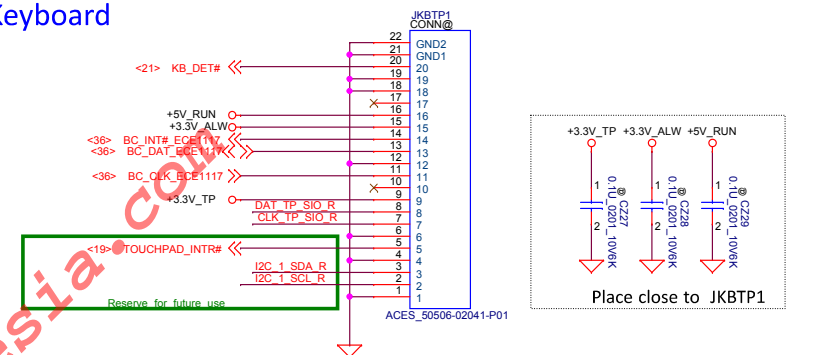
Title			E-Dock	Rev	0.1
Size	Document Number				
			LA-C841P		
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Touch Pad



Keyboard



Link 50506-02041-P0 DONE

RSMRST circuit

Move to CPU page

@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 25W1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 12MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-BB3 ADDA

@Speak

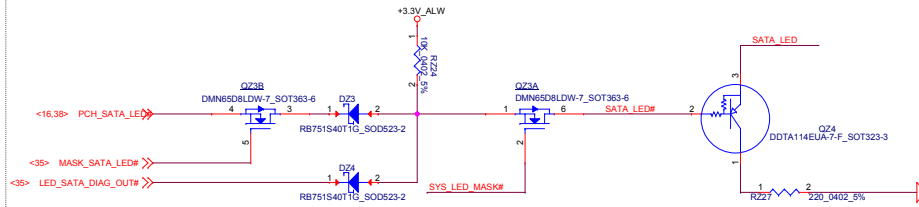
Part Number	Description
SK230003Q0L	SPK PACK 2JX 2.0W 4 OHM FG

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Title	
Keyboard	
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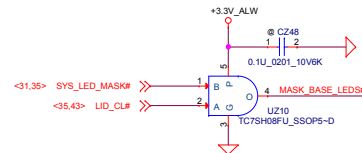
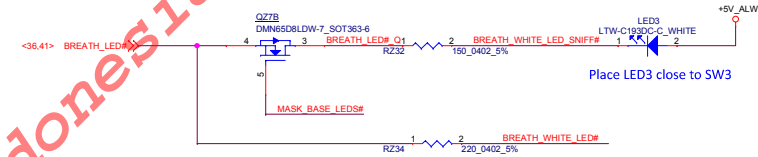
HDD LED solution for White LED



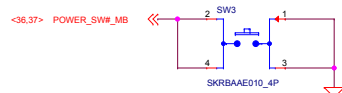
Battery LED



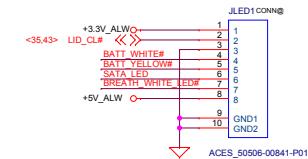
Breath LED



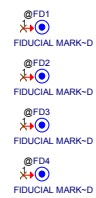
POWER & INSTANT ON SWITCH



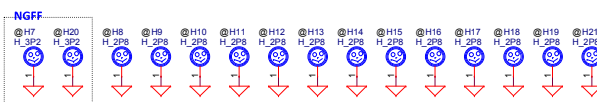
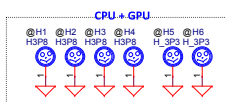
LED board CONN



Fiducial Mark



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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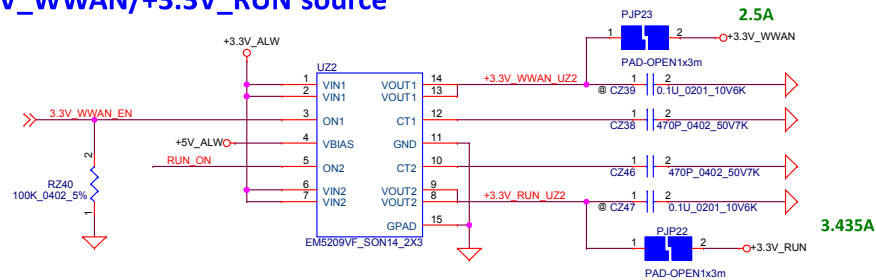
PAD, LED

LA-C841P

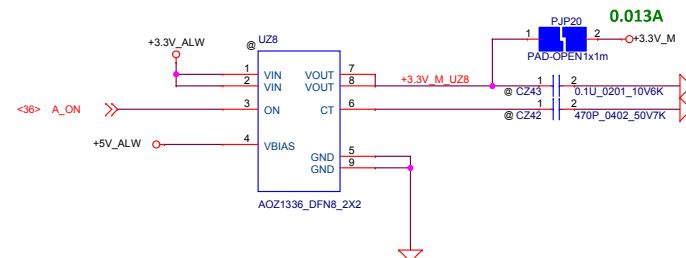
Size Document Number Rev 0.1

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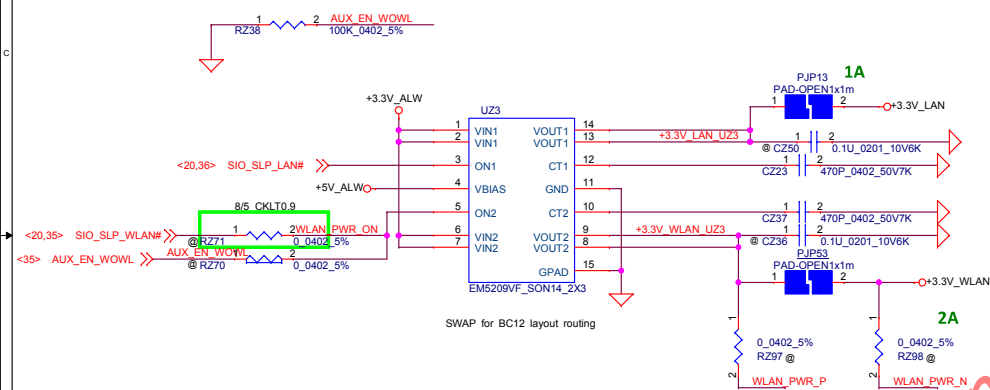
+3.3V_WWAN/+3.3V_RUN source



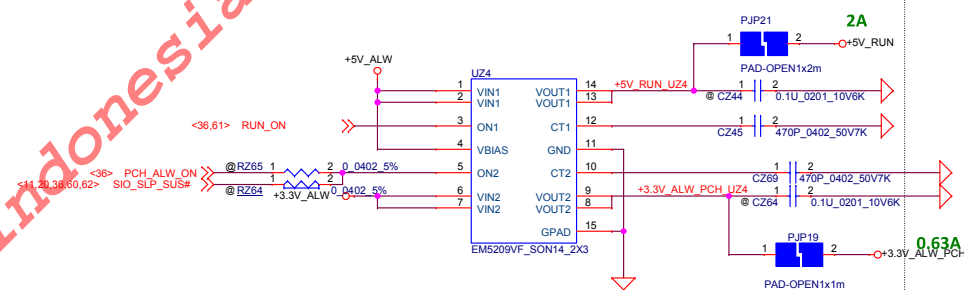
+3.3V_M source



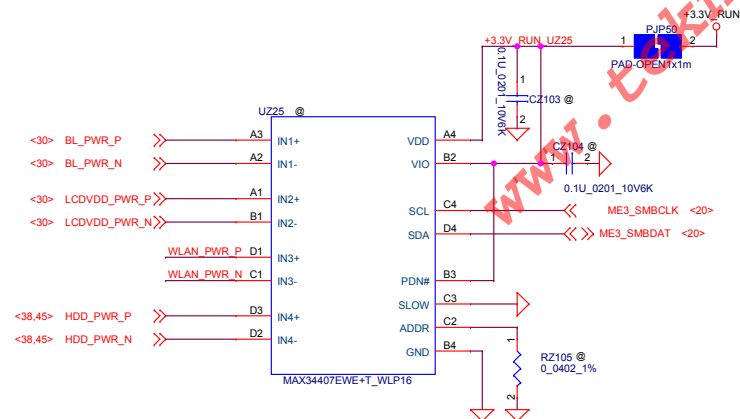
+3.3V_WLAN/+3.3V_LAN source



+5V_RUN/+3.3V_ALW_PCH source



+3.3V_SUS source



Move to USH/B

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Power control

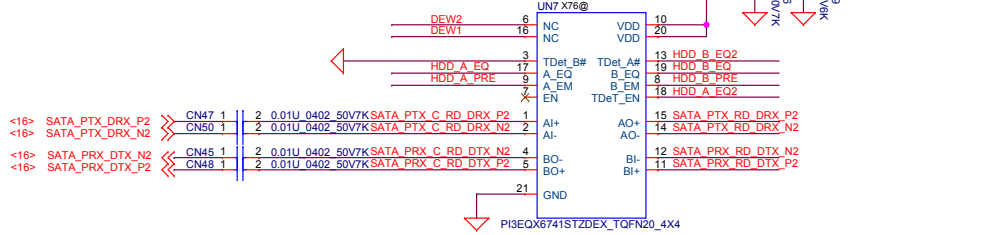
LA-C841P

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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDet_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater

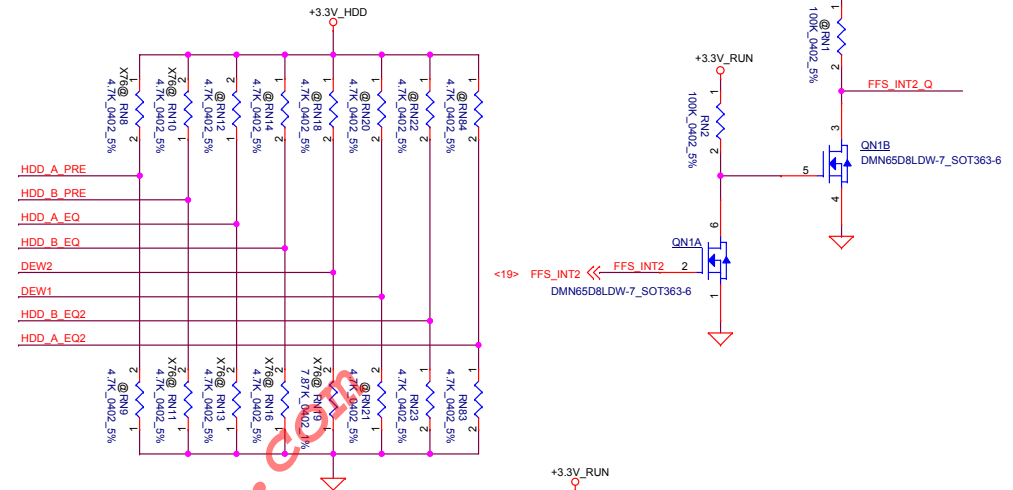
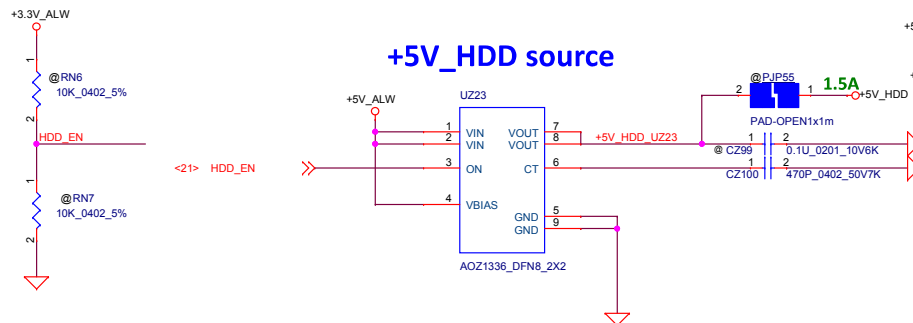


		HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom	PI3EQX6741ST	NC	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI	SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade	PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

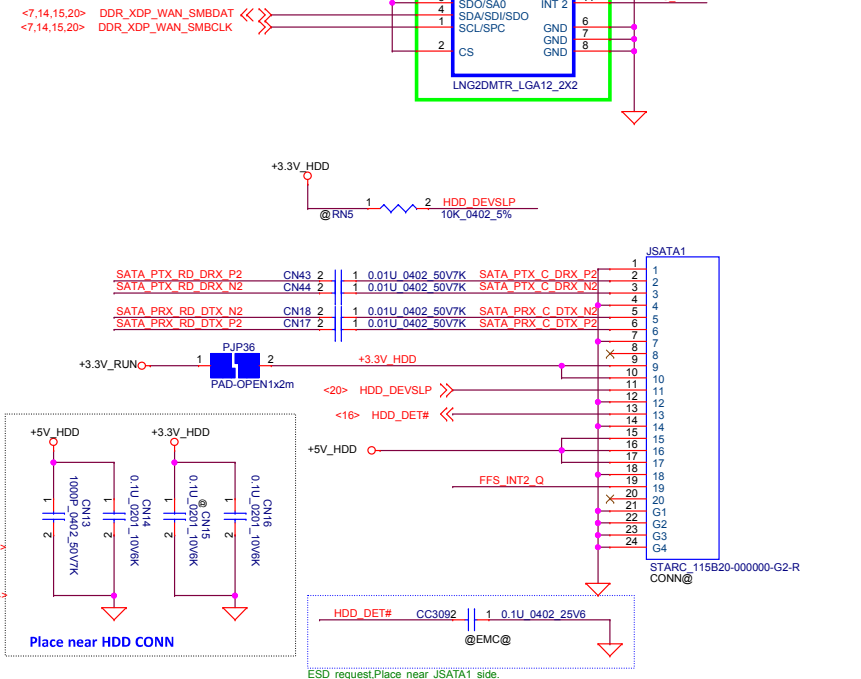
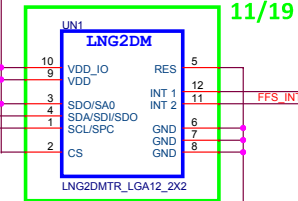
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2					
		EQ1					
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

* red color is current setting

+5V_HDD source



Free Fall Sensor



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Compal Electronics, Inc.	
HDD CONN	
LA-C841P	
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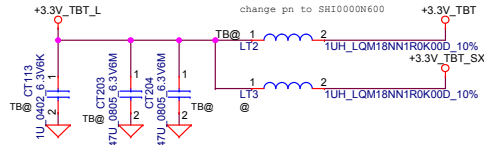
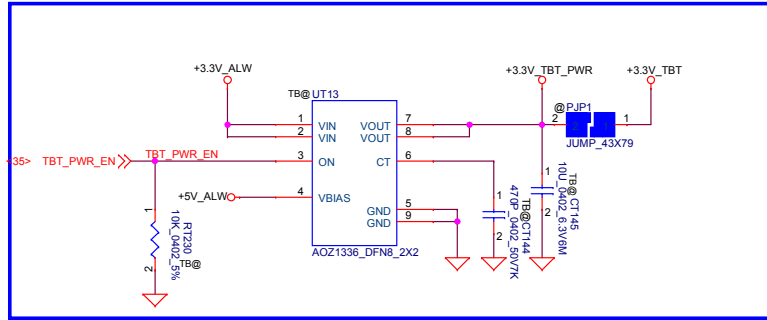
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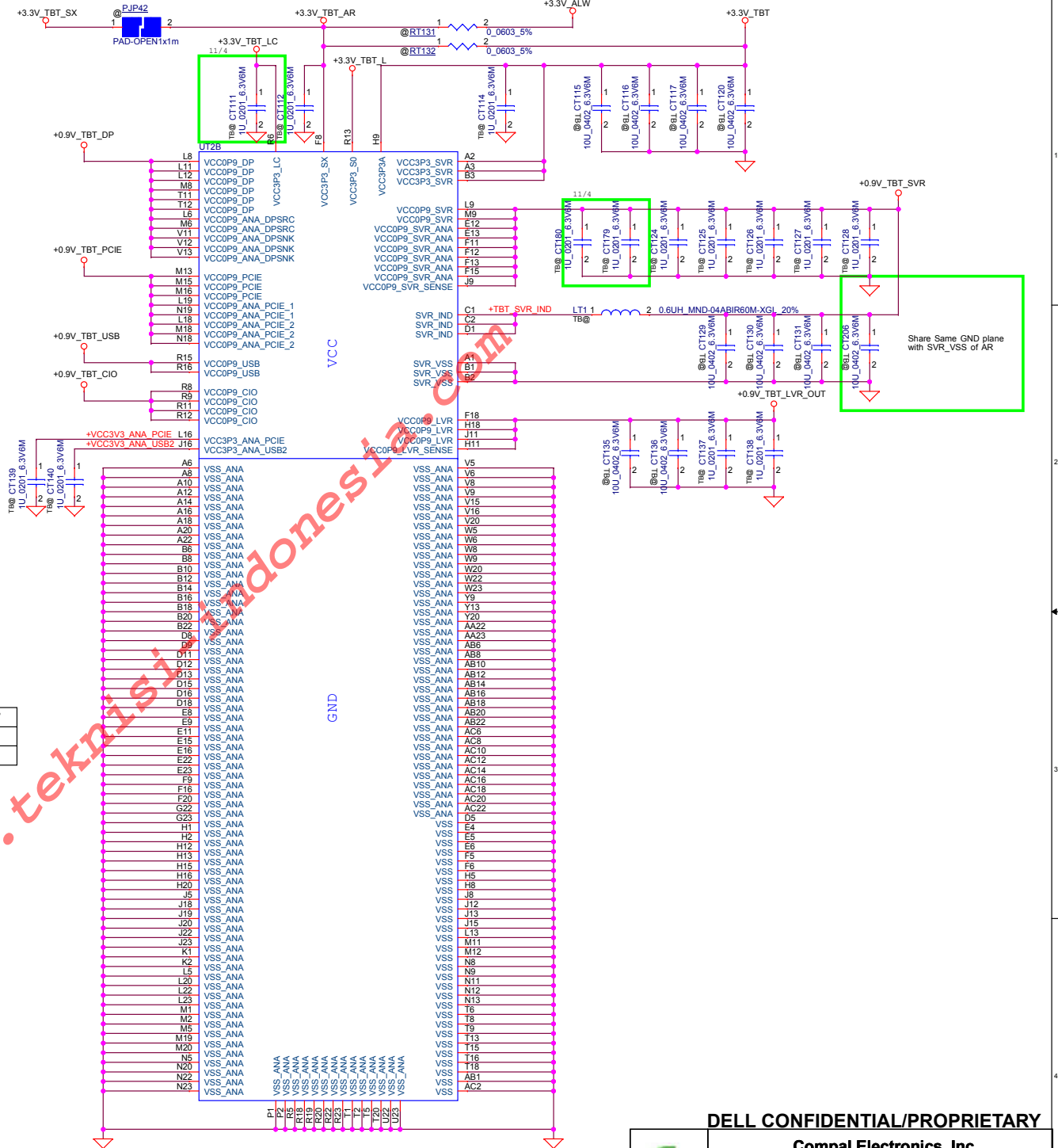
Rev	0.1
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TBT Power circuit



UT2 chip version	POP
A1 B1	LT2
B0	LT3



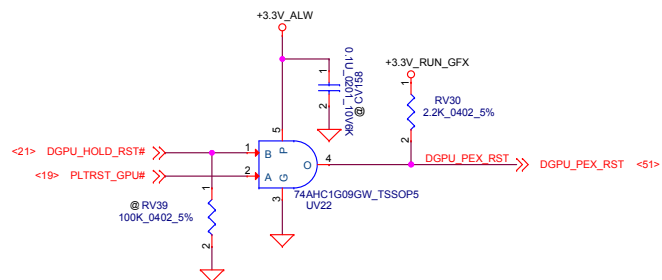
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		TBT-AR-SP(2/4) PWR,VSS	
Title	Size	Document Number	Rev 0.1
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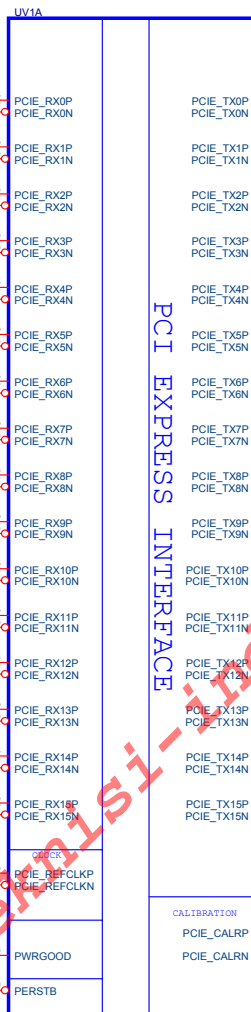
<6> PEG_CTX_C_GRX_P[0..15]>> PEG_CTX_C_GRX_P[0..15]
<6> PEG_CTX_C_GRX_N[0..15]>> PEG_CTX_C_GRX_N[0..15]
<6> PEG_CRX_GTX_P[0..15]>> PEG_CRX_GTX_P[0..15]
<6> PEG_CRX_GTX_N[0..15]>> PEG_CRX_GTX_N[0..15]

<18> CLK_PEG_P0 >> CLK_PEG_P0
<18> CLK_PEG_N0 >> CLK_PEG_N0
RV306 1 2 1K_0402_1%
DGPU_PEX_RST @RV23 1 2 0_0402_5%
RV30 1 2 2.2K_0402_5%
RV39 1 2 100K_0402_5%
74AHC1G09GW-TSSOP5
UV22



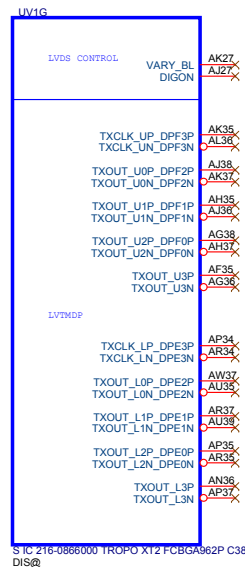
PCI EXPRESS INTERFACE

PEG_CTX_C_GRX_P0	AA38	PCIE_RX0P	Y33	PEG_CRX_C_GTX_P0	0.22U 0402 10V6K 1	2	CV30	PEG_CRX_GTX_P0
PEG_CTX_C_GRX_N0	Y37	PCIE_RX0N	Y32	PEG_CRX_C_GTX_N0	0.22U 0402 10V6K 1	2	CV25	PEG_CRX_GTX_N0
PEG_CTX_C_GRX_P1	Y35	PCIE_RX1P	W33	PEG_CRX_C_GTX_P1	0.22U 0402 10V6K 1	2	CV33	PEG_CRX_GTX_P1
PEG_CTX_C_GRX_N1	W36	PCIE_RX1N	W32	PEG_CRX_C_GTX_N1	0.22U 0402 10V6K 1	2	CV24	PEG_CRX_GTX_N1
PEG_CTX_C_GRX_P2	W38	PCIE_RX2P	U33	PEG_CRX_C_GTX_P2	0.22U 0402 10V6K 1	2	CV20	PEG_CRX_GTX_P2
PEG_CTX_C_GRX_N2	V37	PCIE_RX2N	U32	PEG_CRX_C_GTX_N2	0.22U 0402 10V6K 1	2	CV32	PEG_CRX_GTX_N2
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PEG_CTX_C_GRX_N3	U36	PCIE_RX3N	U29	PEG_CRX_C_GTX_N3	0.22U 0402 10V6K 1	2	CV34	PEG_CRX_GTX_N3
PEG_CTX_C_GRX_P4	U38	PCIE_RX4P	T33	PEG_CRX_C_GTX_P4	0.22U 0402 10V6K 1	2	CV1006	PEG_CRX_GTX_P4
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PEG_CTX_C_GRX_P13	H35	PCIE_RX13P	J33	PEG_CRX_C_GTX_P13	0.22U 0402 10V6K 1	2	CV1023 Tropol	PEG_CRX_GTX_P13
PEG_CTX_C_GRX_N13	G36	PCIE_RX13N	J32	PEG_CRX_C_GTX_N13	0.22U 0402 10V6K 1	2	CV1024 Tropol	PEG_CRX_GTX_N13
PEG_CTX_C_GRX_P14	G38	PCIE_RX14P	K30	PEG_CRX_C_GTX_P14	0.22U 0402 10V6K 1	2	CV1021 Tropol	PEG_CRX_GTX_P14
PEG_CTX_C_GRX_N14	F37	PCIE_RX14N	K29	PEG_CRX_C_GTX_N14	0.22U 0402 10V6K 1	2	CV1020 Tropol	PEG_CRX_GTX_N14
PEG_CTX_C_GRX_P15	F35	PCIE_RX15P	H33	PEG_CRX_C_GTX_P15	0.22U 0402 10V6K 1	2	CV1026 Tropol	PEG_CRX_GTX_P15
PEG_CTX_C_GRX_N15	E37	PCIE_RX15N	H32	PEG_CRX_C_GTX_N15	0.22U 0402 10V6K 1	2	CV1025 Tropol	PEG_CRX_GTX_N15



SIC 216-0886000 TROP0 X12 FCBGA962P C38

DIS@



SIC 216-0886000 TROP0 X12 FCBGA962P C38
DIS@

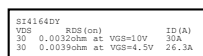
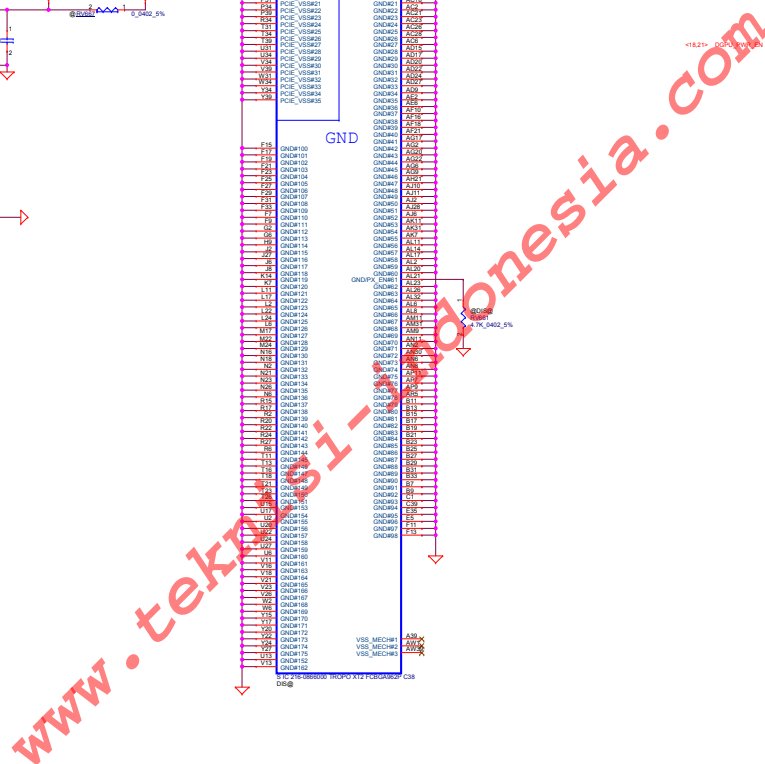
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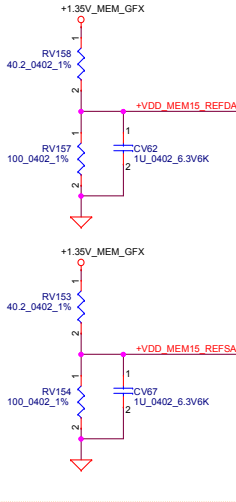
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Size	Document Number	LA-C841P	Rev 0.1
Date:	Tuesday, September 08, 2015	Sheet 50 of 74	

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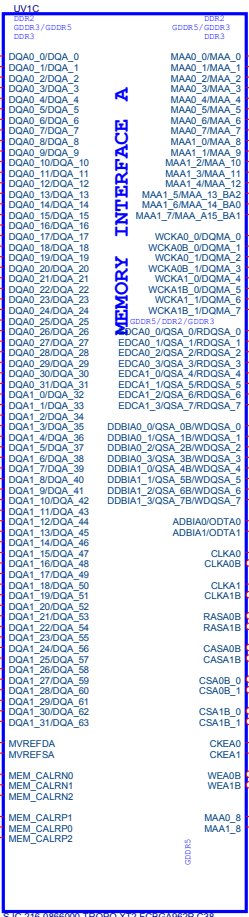
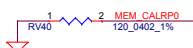


<55> DQA0_0..31 <<>> DQA0_0..31
<55> DQA1_0..31 <<>> DQA1_0..31
<55> MAA0_0..8 <<>> MAA0_0..8
<55> MAA1_0..8 <<>> MAA1_0..8
<55> EDCA0_0..3 <<>> EDCA0_0..3
<55> EDCA1_0..3 <<>> EDCA1_0..3
<55> DBIA0_0..3 <<>> DBIA0_0..3
<55> DBIA1_0..3 <<>> DBIA1_0..3

Place close to UV1



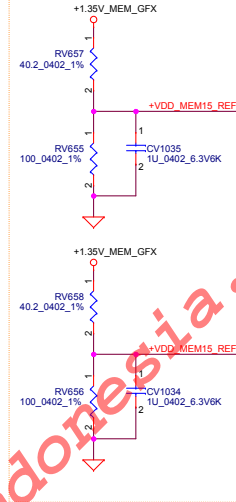
+VDD MEM15_REFDA
+VDD MEM15_REFSB



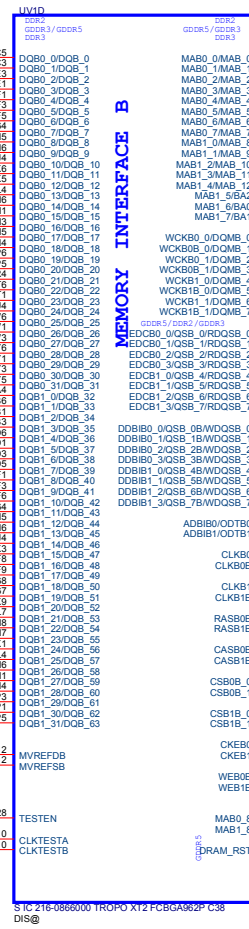
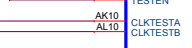
SIC 216-0866000 TROPX12 FCBGA902P C38 DIS@

<56> DOB0_0..31 <<>> DOB0_0..31
<56> DOB1_0..31 <<>> DOB1_0..31
<56> MAB0_0..8 <<>> MAB0_0..8
<56> MAB1_0..8 <<>> MAB1_0..8
<56> EDCB0_0..3 <<>> EDCB0_0..3
<56> EDCB1_0..3 <<>> EDCB1_0..3
<56> DBIB0_0..3 <<>> DBIB0_0..3
<56> DBIB1_0..3 <<>> DBIB1_0..3

Place close to UV1

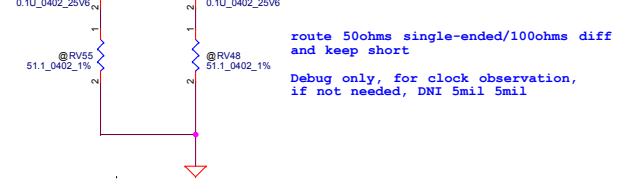
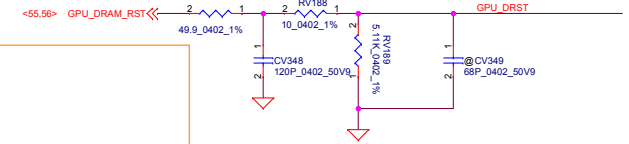


+VDD MEM15_REFDA
+VDD MEM15_REFSB



SIC 216-0866000 TROPX12 FCBGA902P C38 DIS@

Place RV187-RV189, CV348, CV349 close to UV1 within 1000mil



route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil

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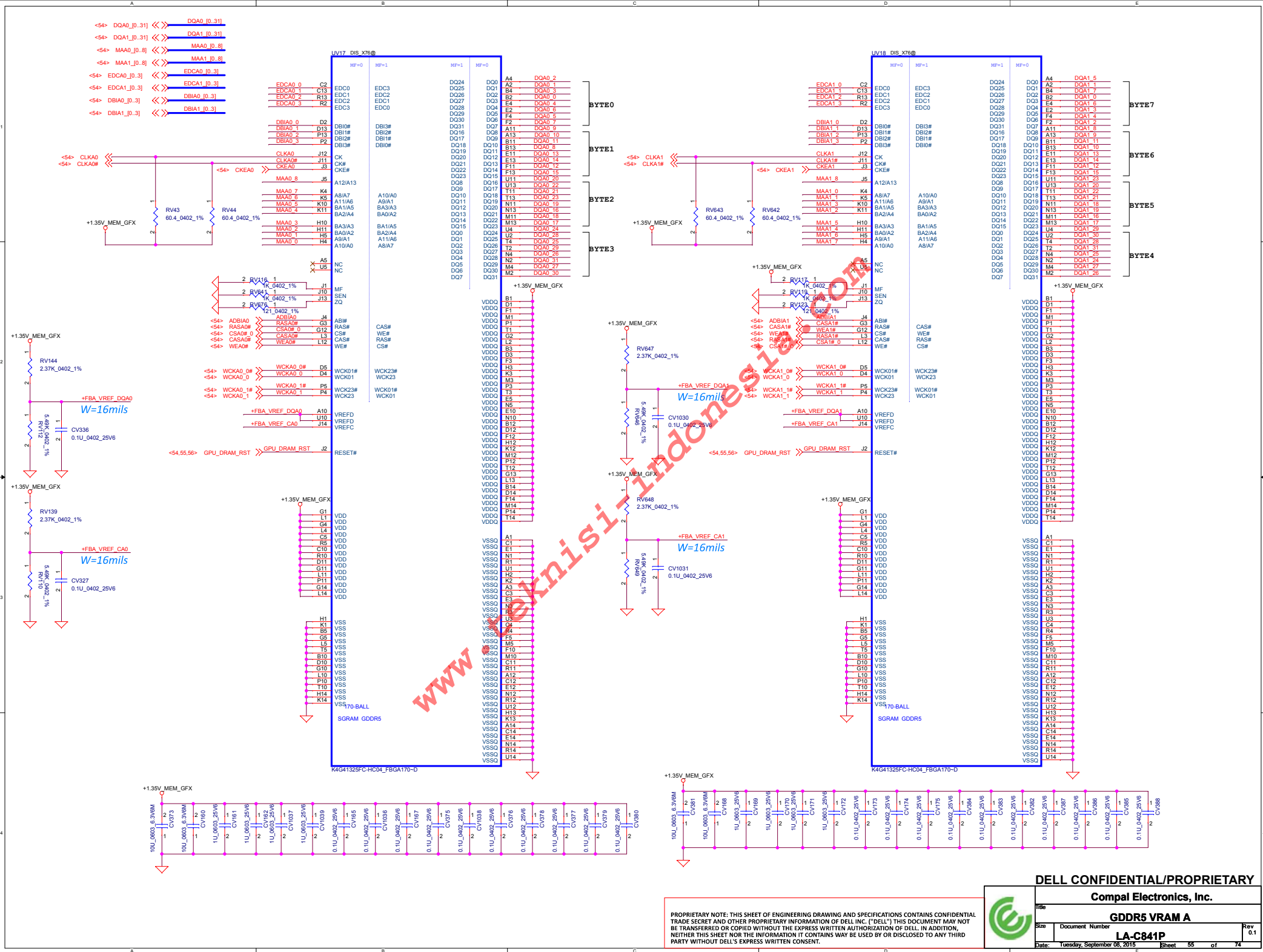
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Title		Meso-MEM Interface A	
Size	Document	Number	Rev
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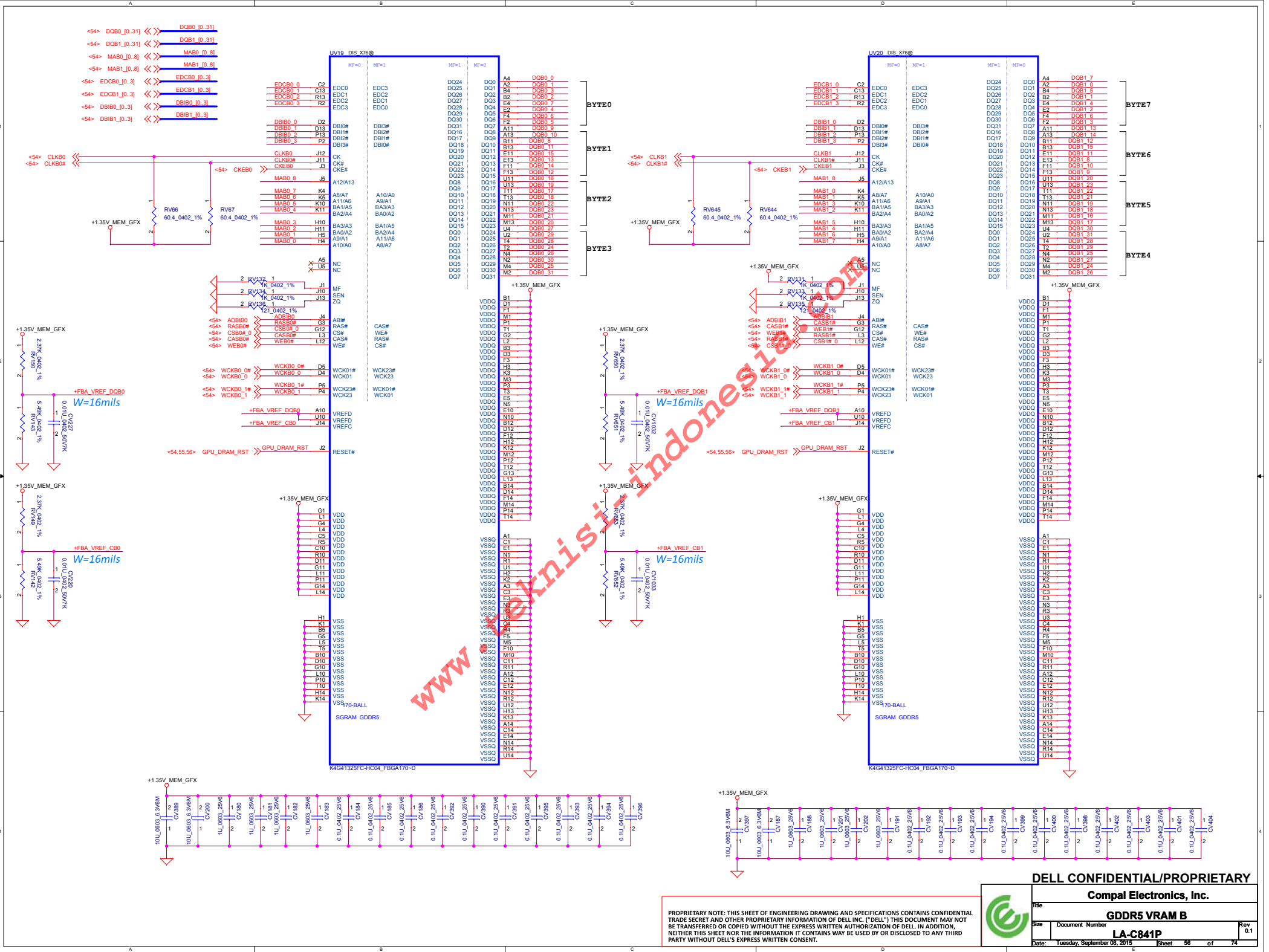
Compal Electronics, Inc.

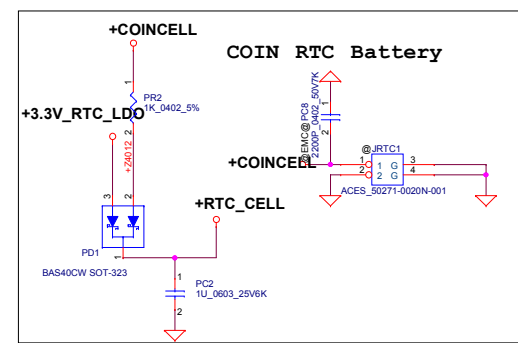
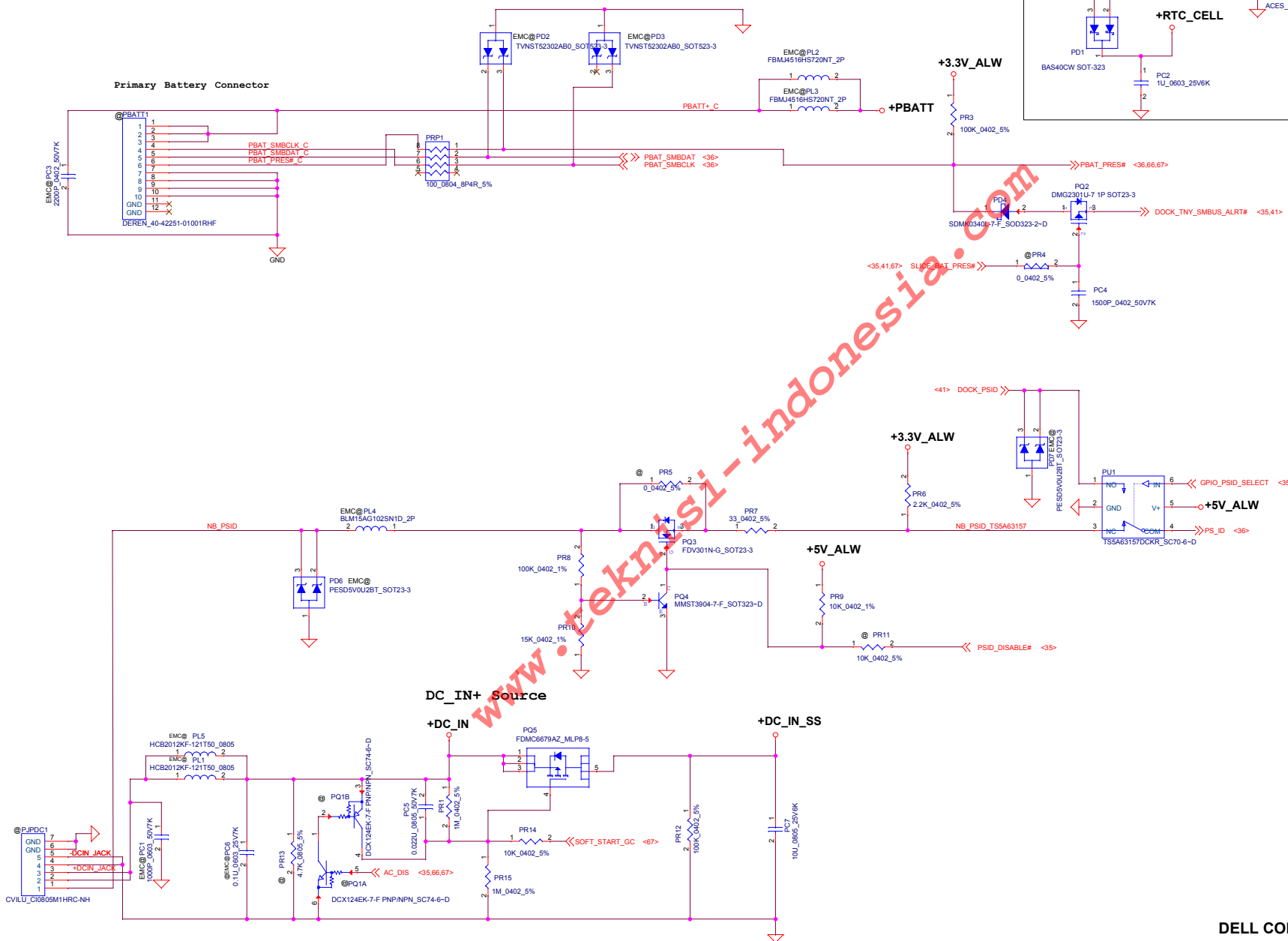
GDDR5 VRAM A

LA-C841P

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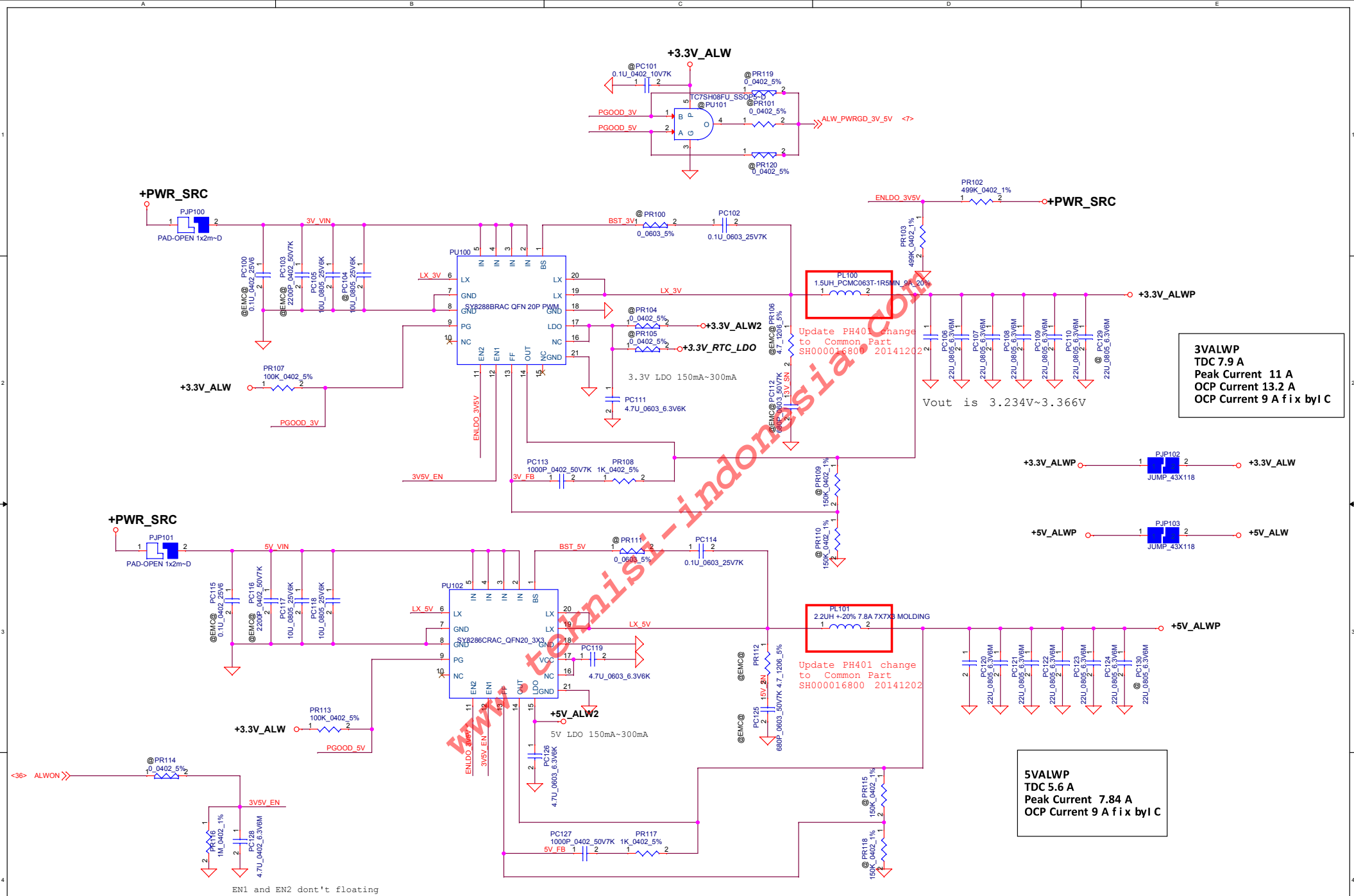




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+DCIN		+DCIN	
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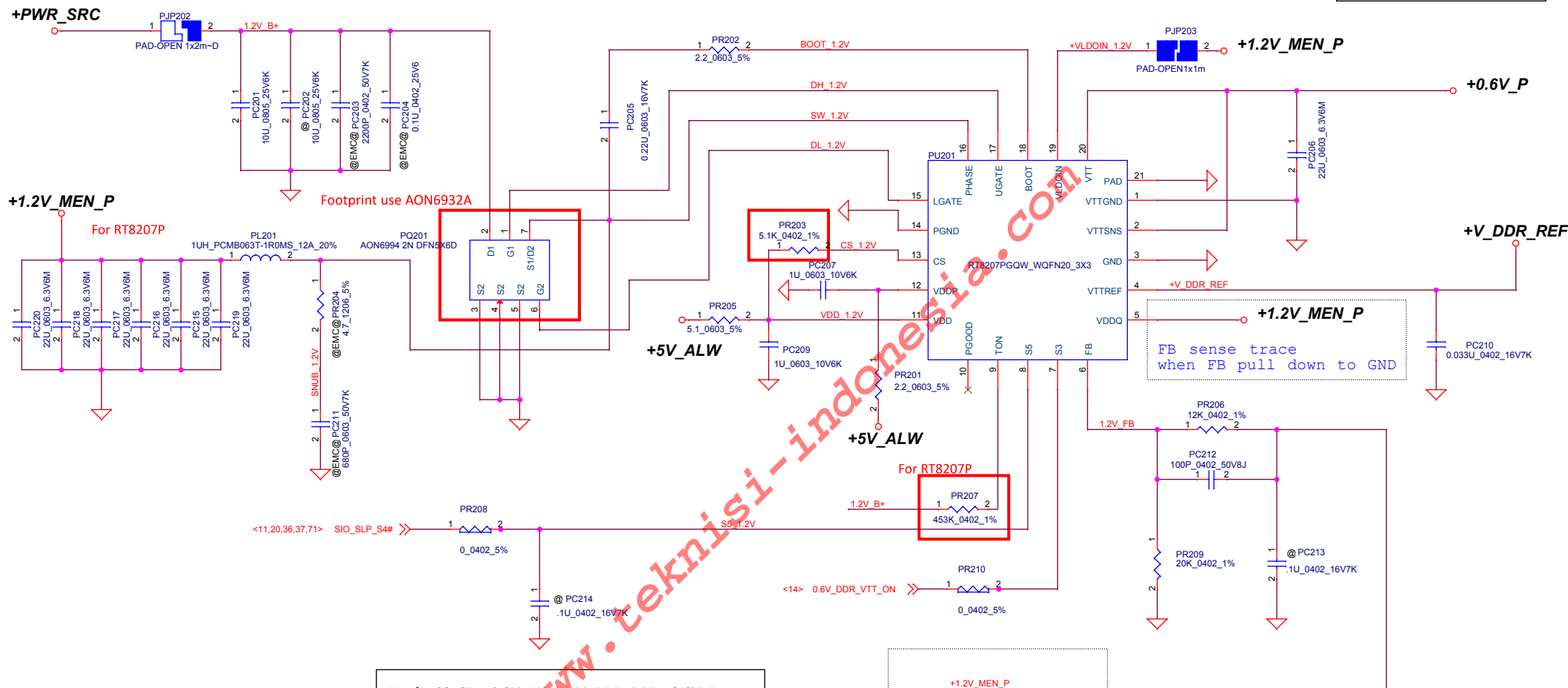


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Title		
+5V_ALW/3.3V_ALW		
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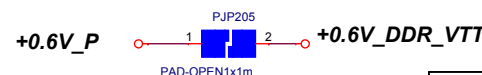
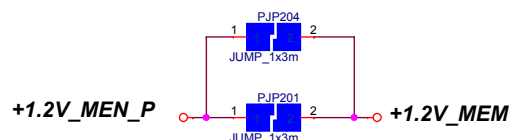
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0.6Volt +/- 5%
TDC 0.787 A
Peak Current 1.1 A
OCP Current 2.6 A f i x byl C



Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

+1.2V_MEM
TDC 8.75 A
Peak Current 12.25 A
OCP Current 14.7A
TYP MAX
H/S Rds(on) 6.8mohm , 8.6mohm
L/S Rds(on) 2.8mohm , 3.5mohm
Choke DCR 3.0mohm , 3.5mohm



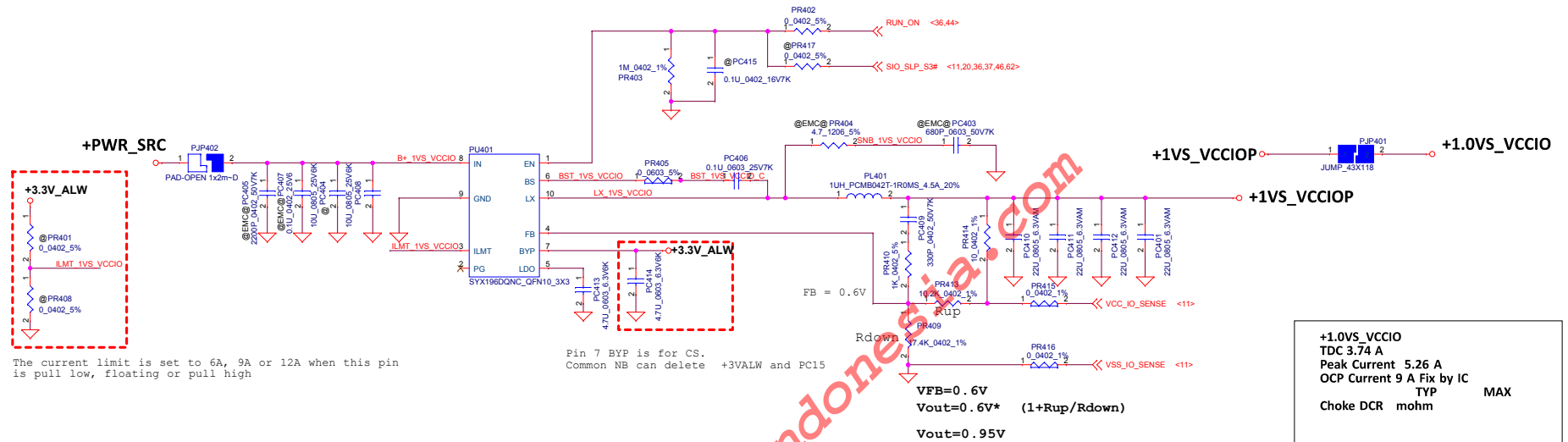
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Title		
+1.2V MEN/+0.6V DDR VTT		
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

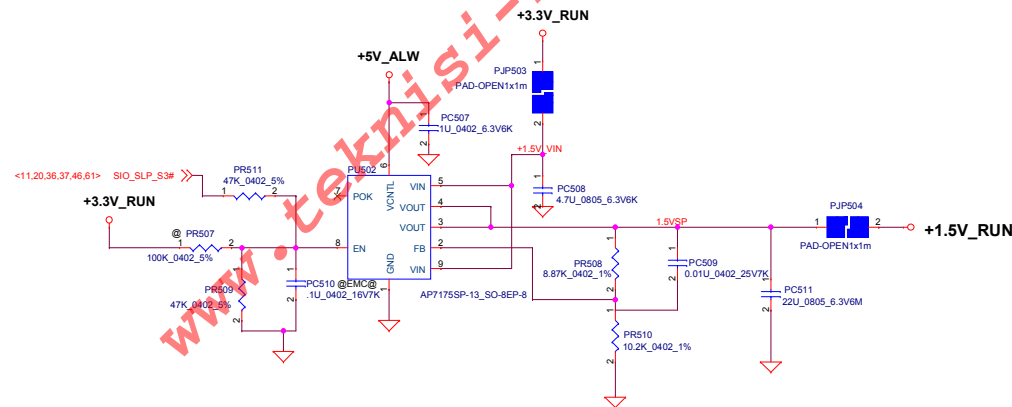
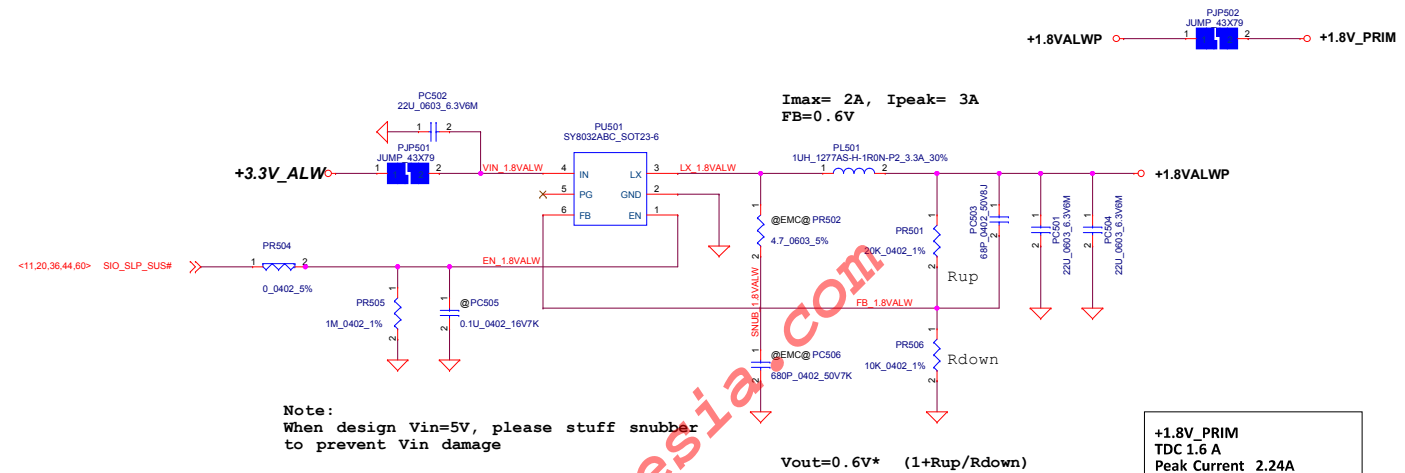
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

+1.0VS_VCCIO
TDC 3.74 A
Peak Current 5.26 A
OCP Current 9 A Fix by IC
Choke DCR mohm
TYP MAX

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Compal Electronics, Inc.	
+1VS_VCCIO	
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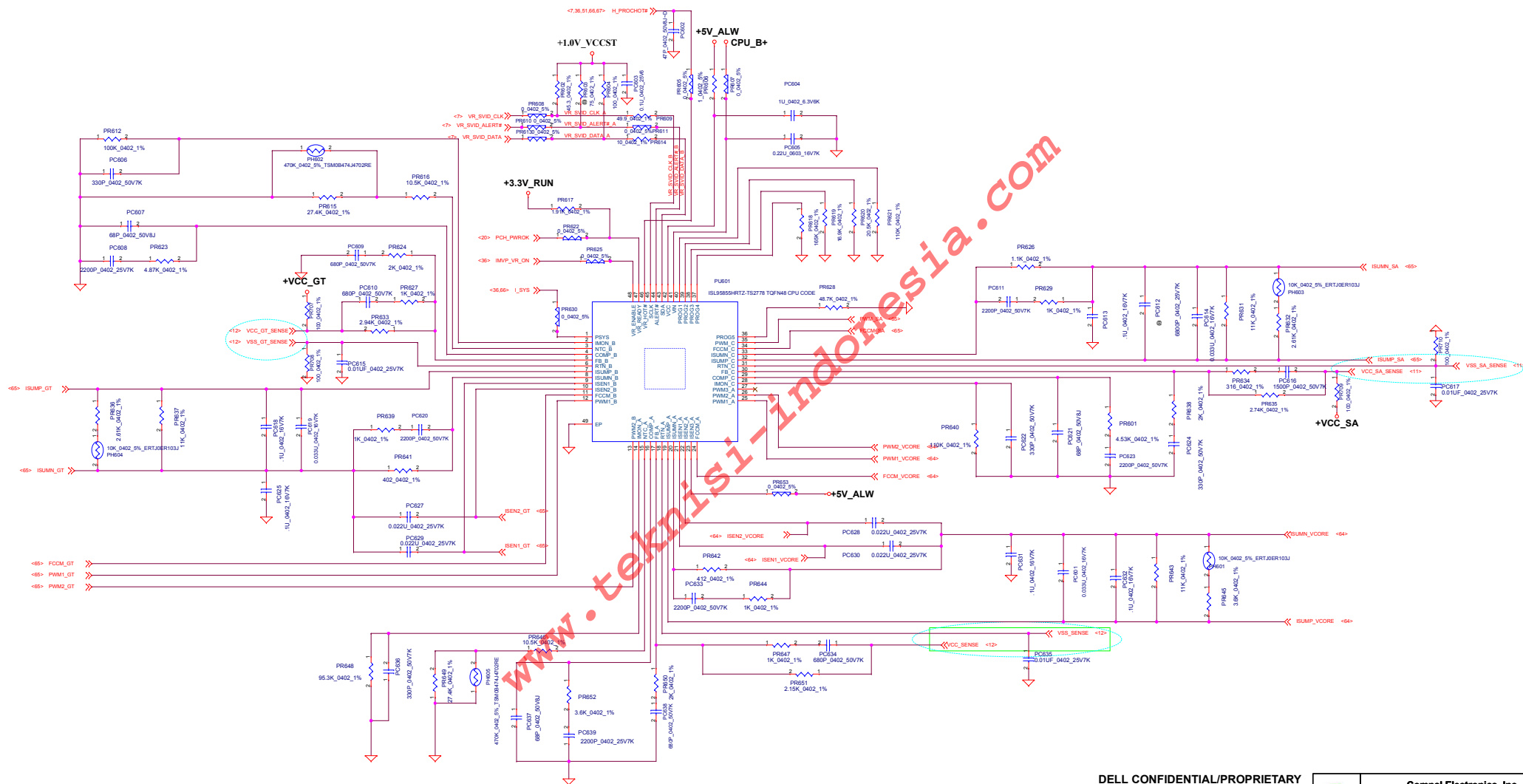
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		+1.8VALWP/+1.5VSP	
Size	Document Number	LA-C841P	
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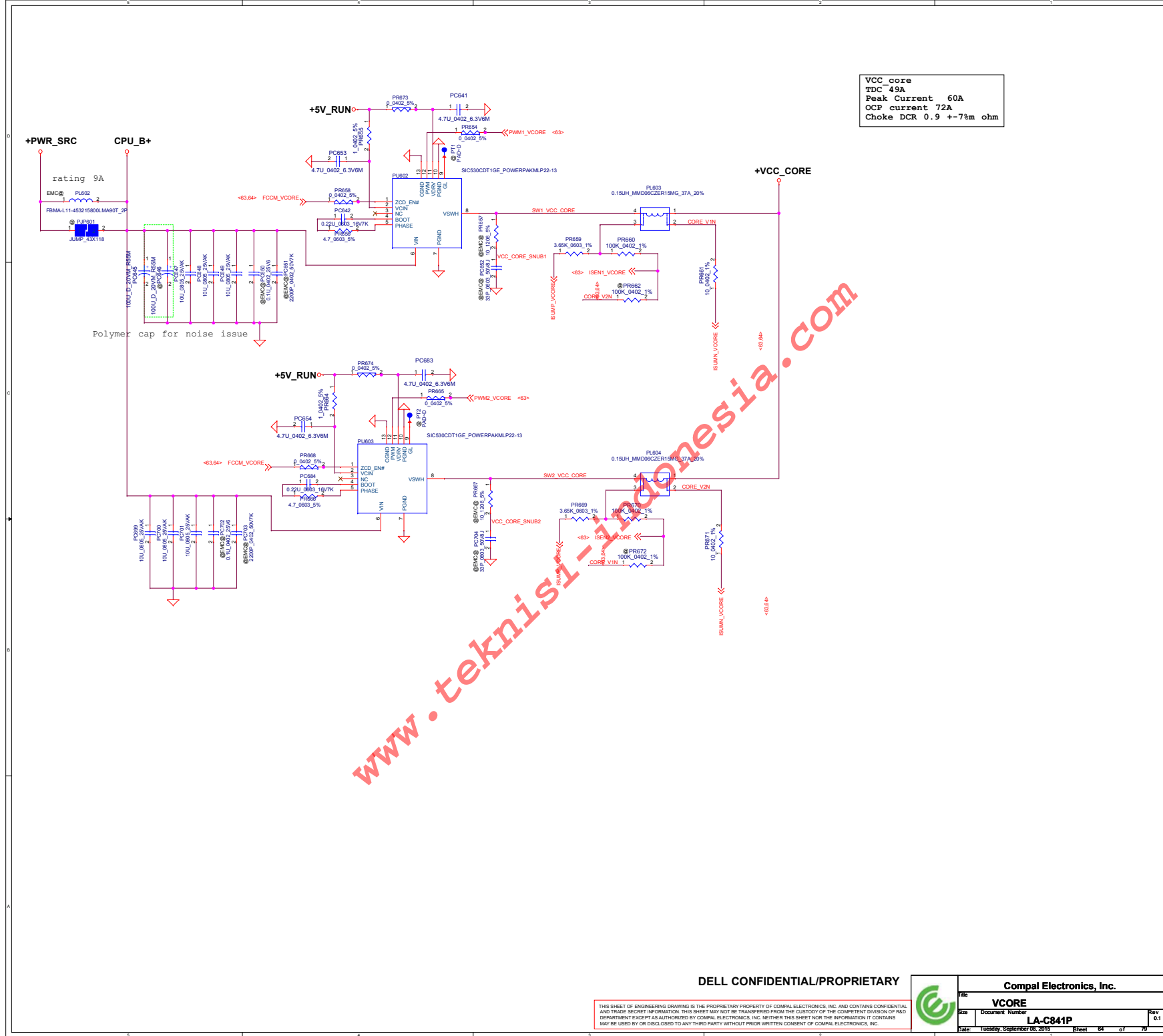
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		VCORE ISL95855	
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001	LA-C841P	001	01
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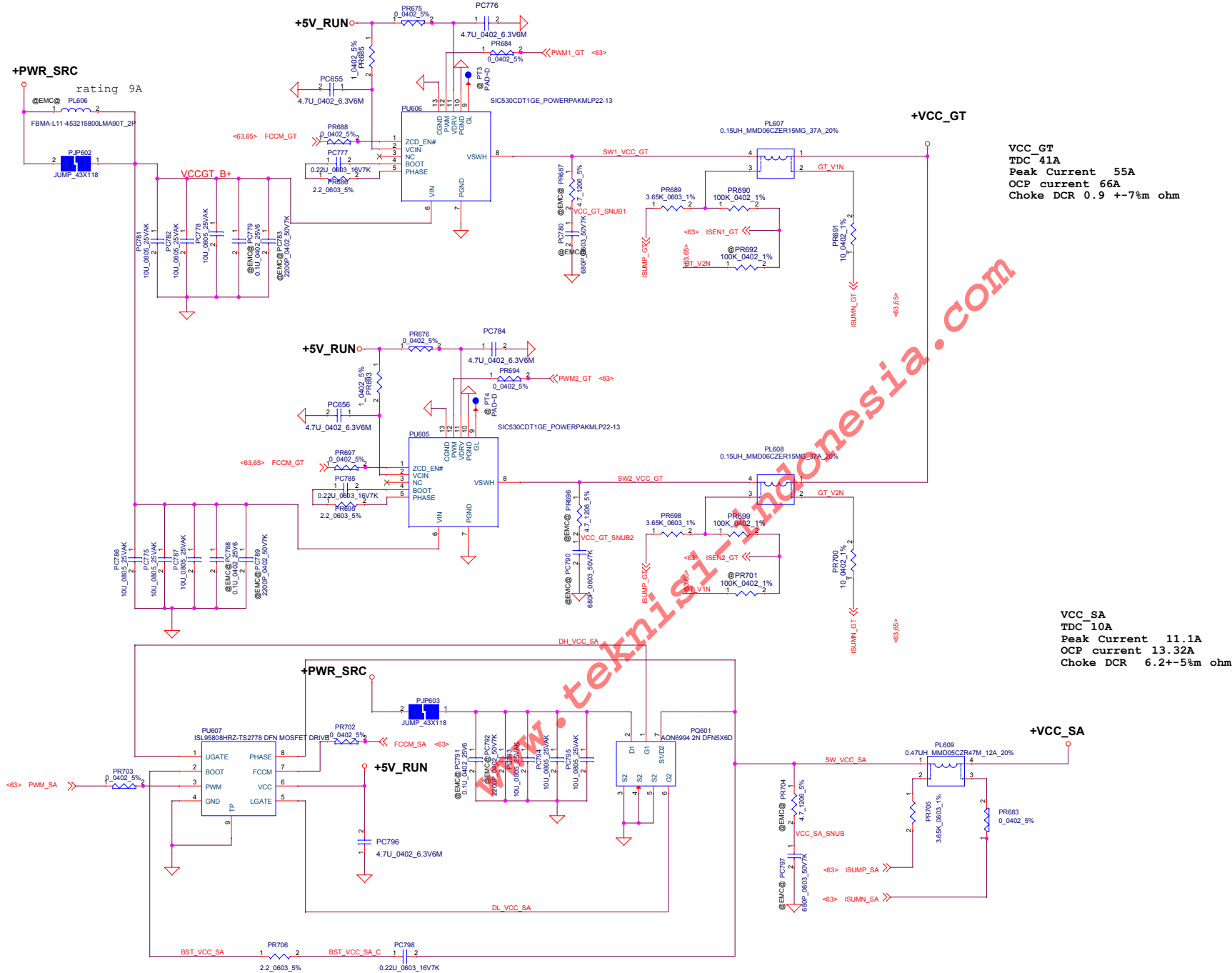


VCC_core
TDC 49A
Peak Current 60A
OCP current 72A
Choke DCR 0.9 +-7% ohm

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Compal Electronics, Inc.	
File	VCCORE
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VGT_VSA			
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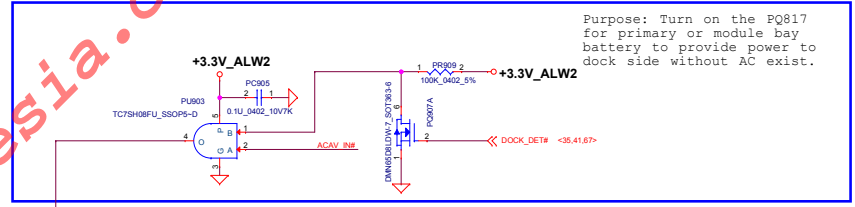
3.3V


10k

1k

10k

0.5-1.5V



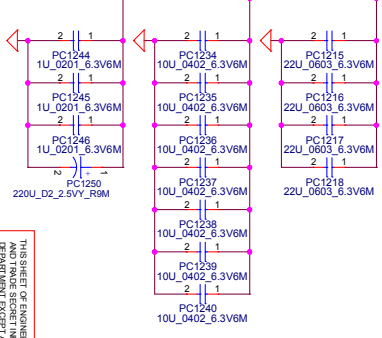
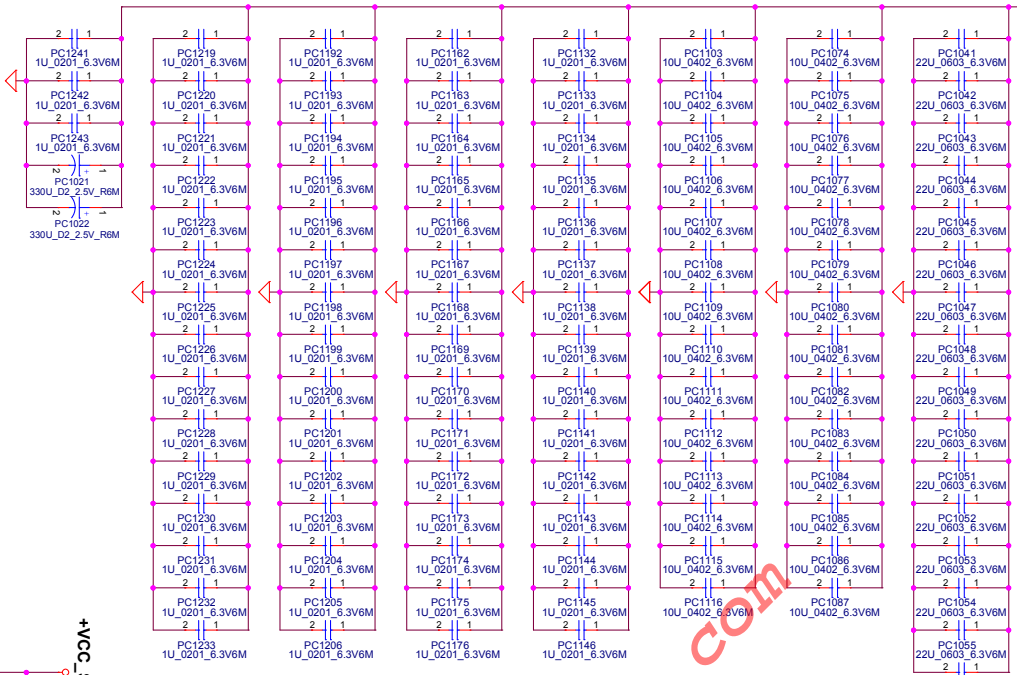
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VCC CORE Place on CPU
Back Side:
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side:
22U_0603 * 8 pcs+330U_D2*2 pcs

VCC CP Place on CPU
Back Side:
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side:
22U_0603 * 12 pcs +470U_D2*2 pcs

VCC CORE Place on CPU
Back Side:
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side:
22U_0603 * 2 pcs + 220U_D2*1 pcs



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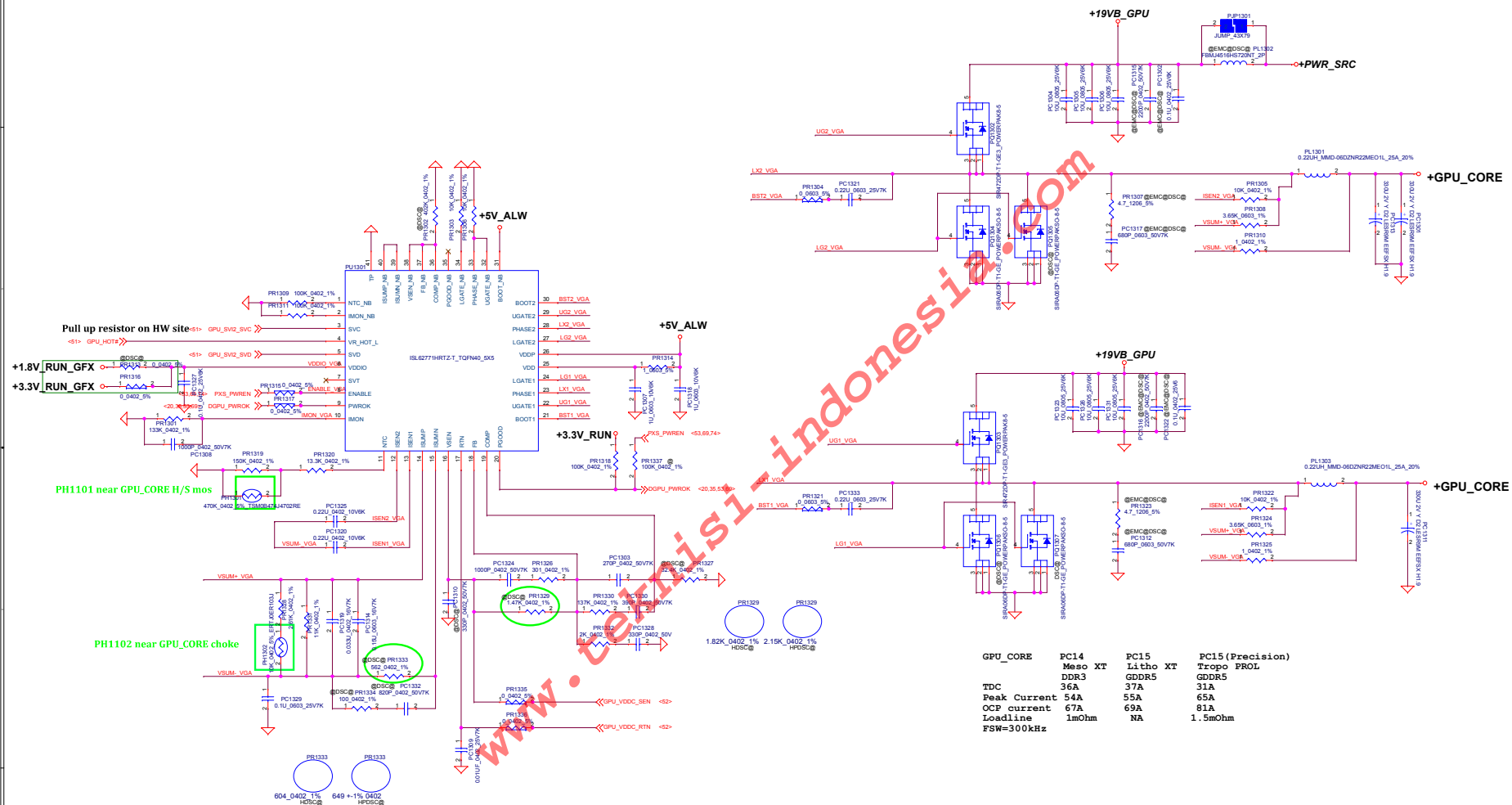
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LA-C841P

Rev 0.1

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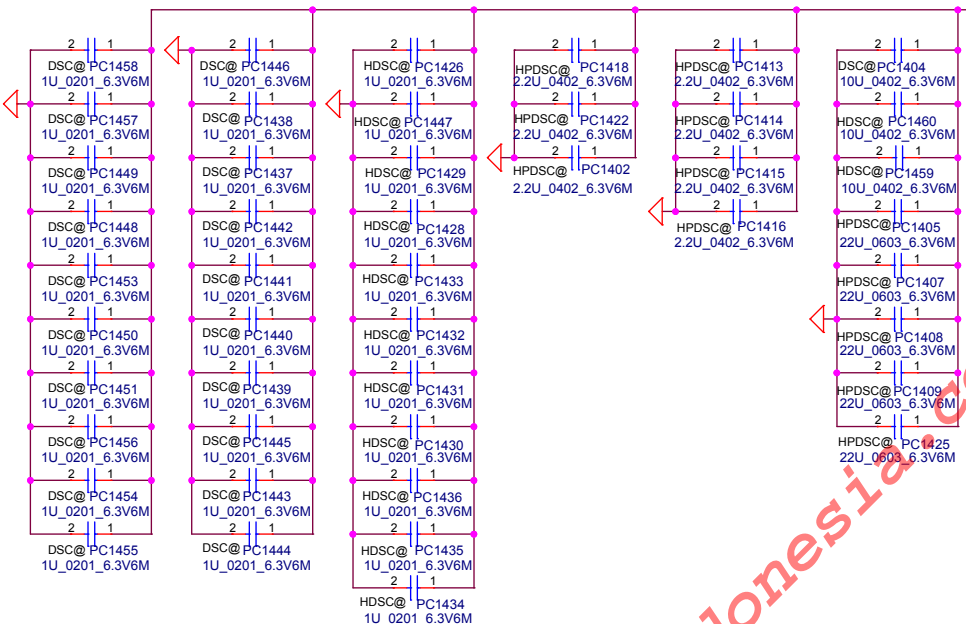


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+GPU_CORE	
Rev	6.1
Document Number	LA-C841P
Date	Wednesday, September 16, 2015
Rev	6.1

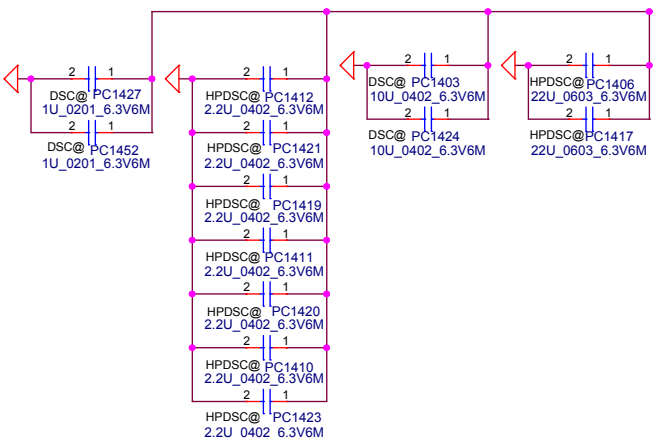
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+GPU_CORE



AMD
Tropo
PROL(P)
VDDC
5*22 uF
1*10 uF
7*2.2 uF
20*1 uF
VDDCI
2*22 uF
2*10 uF
7*2.2 uF
2*1 uF
AMD
Litho XT
VDDC
4*10 uF
30*1 uF
VDDCI
1*10 uF
3*1 uF

+0.9V_VDDCI



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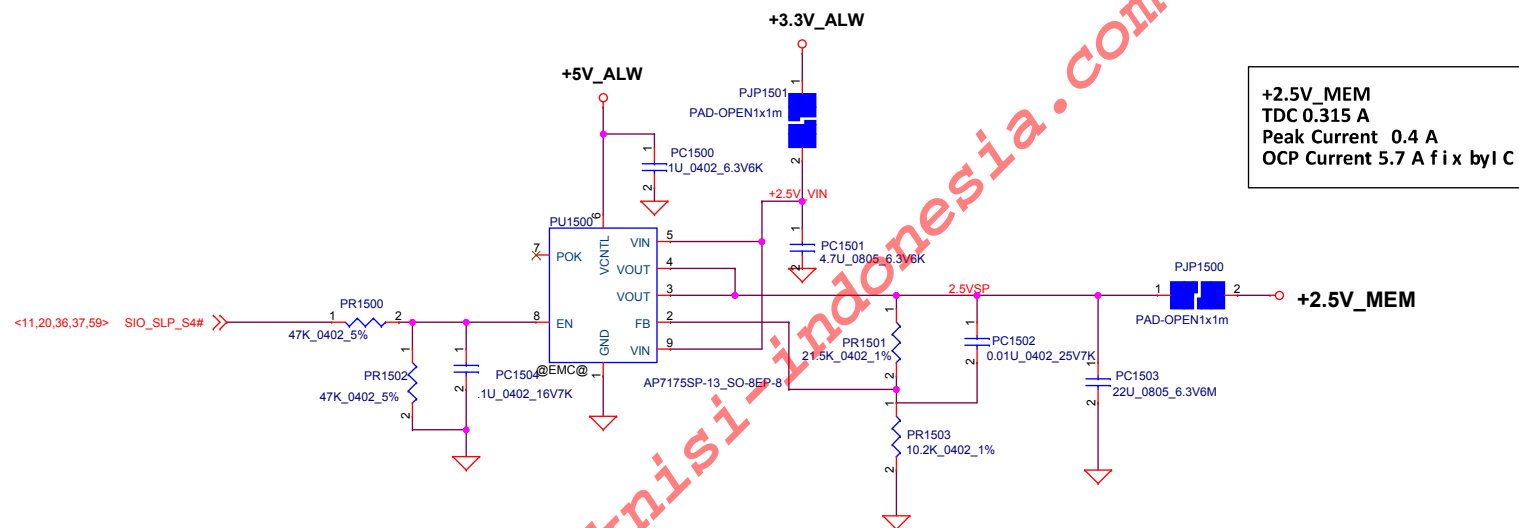
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GPU DECOUPLING

Size Document Number LA-C341P Rev 0.1

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Title	+2.5V_MEM	
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Compal Electronics, Inc.

ParkCity_TypeC_PD

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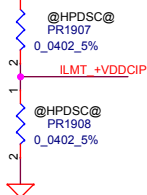
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ParkCity TypeC PD
LA-C841P
 Date: Tuesday, September 08, 2015 Sheet 73 of 79 Rev. 0

+PWR_SRC

PJP1901
PAD-OPEN 1x2m-D

+3.3V_ALW



+0.9V_VDDCI

TDC 7 A

Peak Current 10.5 A

OCP Current 12 A Fix by IC

TYP

MAX

Choke DCR 11.0mohm, 12.0mohm

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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PU1901
SYX198DQNC_QFN10_3X8

EN +VDDCIP

+3.3V_ALW

+0.9V_VDDCIP

PJP1902
JUMP_43X118

+0.9V_VDDCI

+0.9V_VDDCIP

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Version Change List (P. I. R. List)

Item Page# Title Date Request Owner

Issue Description

Solution Description

Rev.

1	74	Type-C PD	3/23	Compal	Ensure the DCIN_ACOK voltage level can not be divide.	Change the PR1865 PR1861 to 10K	X01
2	74	Type-C PD	3/23	Compal	Ensure the S6 Mosfet turn on sequency after PQ802 turn off to avoid the +SDC IN oscillate to cause audible noise when with M/B AC and TypeC AC then pulg out M/B AC	Change the PR1806 to 40.2K	X01
3	74	Type-C PD	3/23	Compal	Voiaad the +Vbus_DC_ss leak to +PWR_SRC when tininty dock with AC and M/B without AC	Depop PD1815 and PR1915	X01
4	74	Type-C PD	3/23	Compal	Reserve Dock AC_OK circuit to turn off the S8 and S9 when trinity dock plug in AC	Reserve PR1921 PD1817 PR1922 PR1926 PR1925 PR1923 PR1924 PD1818	X01
5	67	Cherger	3/23	Compal	Provide the charger operate voltage when M/B just has TypeC AC only	Add PD804	X01
6	67	Cherger	3/23	Compal	Avoid the +SDC IN oscillation to cause audible noise when system with M/B AC and TypeC AC then plug out M/B AC	Add PD805 PR843 PR842 PQ812 PR845 PR844 PR841 PR838 PQ811 PR839 PR840	X01
7	68	Selector	3/23	Compal	Avoid the +SDC IN oscillation to cause audible noise when system with E-DOCK AC and TypeC adapter then plug out E-DOCK AC	Add PD906 PR943 PR944 PQ999 PR942 PR940 PR941	X01
8	74	Type-C PD	4/10	Compal	Reserve circuit for charger adapter monitor function when system with trinity dock AC only	Add PR1927 PR1928 PQ1826 PQ1823 PR1885 PR1888 PR1884 PR1886 PR1887 PR1829 PR1832 PQ1818 PR1889 PR1890 PR1891	X02
9	67	Cherger	4/10	Compal	Avoid the +SDC IN oscillation to cause audible noise when system with M/B AC and TypeC AC then plug out M/B AC	Add PR1891 PR1889 PR1890 PR846 PC838 PQ813 PR847 PR848 PQ814 PR849	X02
10	74	Type-C PD	4/10	Compal	Add pull down for OVP circuit to enable OVP initial. Reserve control circuit from GPIO1 and GPIO2 for OVP function enable.	Add PR1927 PR1928 PQ1826 PQ1823 PR1885 PR1888 PR1884 PR1886 PR1887 PR1829 PR1832 PQ1818 PR1889 PR1890 PR1891	X02
11	74	Type-C PD	4/29	Compal	For reduce inrush current when dual AC and single AC (Dell request)	Add PU1805,PU1806,PC1831,PC1832,PQ1828,,PQ1827,PR1929,PR1930,PR1931,PR1932,PR1933	X02
12	74	Type-C PD	6/11	Compal	For reduce inrush current (PQ1805 close late), change method for S6 control	Depop PR1805,PR1807,PR1811 Add PU1807,PR1934 PC1833	X02
13	68	Selector	6/11	Compal	add 1 GPIO to program PROCHOT_GATE	Add PQ912 PR945 PC909 PU904 PR946 PR947	X02
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1	21	PCH-H(6/9)	2015/02/28	COMPAL	Align PC14 GPIO for Non-DOCK	Reserve RH359 100K Pull down	0.2 (X01)
2	6, 9	+VCC_IO	2015/02/28	COMPAL	PC15 H Can't boot issue	Change +VCC_IO to +1.0VS_VCCIO	0.2 (X01)
3	20, 21	LAN_WAKE#	2015/02/28	COMPAL	LAN_WAKE# shut down auto pwr on issue	Pop RH93, Depop RL70	0.2 (X01)
4	17	PCH-H(2/9)	2015/03/02	COMPAL	DCI (Direct Connect Interface) test	Add RH364, RH365	0.2 (X01)
5	31	LAN	2015/03/02	COMPAL	IEEE EA measurement	Change LL2 ~ LL9 to 2.2 ohm Res (RL71~RL78)	0.2 (X01)
6	36	MEC5085	2015/03/09	COMPAL	AC_PRESENT need PH.	Add RE309 PH to +3.3V_ALW	0.2 (X01)
7	21	VGA	2015/03/09	COMPAL	0.1(X00) VGA no function	PH 2.2K ohm(RH369) to +3.3V_RUN on UH1.BE6 (DDPD_CTRLDATA)	0.2 (X01)
8	46	AR	2015/03/09	COMPAL	AR circuit modify	Add RT212 ~RT221, Reserve RT212 & RT214	0.2 (X01)
9	52	GPU	2015/03/09	COMPAL	Can't have different stencil for different GPU PWR jump	PJP1903 & RV1082, RV1083 Colay	0.2 (X01)
10	46	AR	2015/03/11	COMPAL	AR circuit modify	LSTX and LSRX link to Debug 3 and 4	0.2 (X01)
11	46	AR	2015/03/11	COMPAL	TBT & HDMI Priority	Swap AR DP0 & DP1	0.2 (X01)
12	20	PCH-H(5/9)	2015/03/11	COMPAL	HDD_FALL_INT PH	Add RH355	0.2 (X01)
13	46	AR	2015/03/12	COMPAL	AR circuit modify	Add RT222, RT223, RT224, RT225	0.2 (X01)
14	37	TPM	2015/03/12	COMPAL	TPM circuit modify	Add RZ112, RZ113, Depop RZ108	0.2 (X01)
15	21	PCH-H(6/9)	2015/03/12	COMPAL	DIMM TYPE GPIO	Add RH372	0.2 (X01)
16	26, 27	DP DeMux	2015/03/19	COMPAL	HDMI & DP EA Fail	UV28, UV29 change from Pericom to Parade solution.	0.2 (X01)
17	49	AR	2015/03/02	COMPAL	AR circuit modify	DOCK_AC_OK and SYSTEM_WAKE# link to Debug 1 and 2	0.2 (X01)
18	21	PCH-H(6/9)	2015/03/27	COMPAL	IR_CAM DET# GPIO	IR Camera pin change and new GPIO on GPP_A23, include PU RH373	0.3 (X02)
19	46	TBT AR	2015/03/30	COMPAL	AR ROM PWR RAIL Modify	Remove RT214, RT215; Add PWR Rail +3.3V_TBT_FLASH_R	0.3 (X02)
20	37	USH & TPM2.0	2015/03/30	COMPAL	USH RST#	Add RZ114, RZ115 & Depop, USH RST#	0.3 (X02)
21	47	TBT AR	2015/03/30	COMPAL	Modify AR +3.3V_TBT_SX	DEPOP RT131	0.3 (X02)
22	46	TBT AR	2015/03/30	COMPAL	Add Reset IC for PD_RESET# AR reset must assert after +3.3V_TBT 100us	Add UT23, CT200, CT201, RT232, RT233, RT234, RT235	0.3 (X02)

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24	46	TBT AR	2015/03/30	COMPAL	Vendor recommend add PD_RESET# cap	Add @CT199	0.3 (X02)
25	47	TBT AR	2015/03/31	COMPAL	Give TBT_PWR_EN default value	Add pull down 10k(RT230)	0.3 (X02)
26	*	X'tal	2015/04/01	COMPAL	X'tal EA	Change CE28, CE29 from 33p to 27p Change CH4, CH5 from 18p to 15p Change CH13, CH14 from 22p to 15p Change CV163, CV163 from 6.8p to 10p	0.3 (X02)
27	49	TBT-AR	2015/04/02	COMPAL	AR PD TPS65982 Soft-start pin	Add CT202 0.22u	0.3 (X02)
28	48	TBT-AR	2015/04/02	COMPAL	UT17 LDO source change from +Vbus_1 to +PP_HV	UT17 LDO source change from +Vbus_1 to +PP_HV	0.3 (X02)
29	49	TBT-AR	2015/04/02	COMPAL	AR PD TPS65982 BUSPOWER_N change to VCC1V8D_TBTA_LDO	AR PD TPS65982 BUSPOWER_N change to VCC1V8D_TBTA_LDO	0.3 (X02)
30	30	eDP	2015/04/02	COMPAL	IR CAM Pin Define	NC JIR1 Pin4	0.3 (X02)
31	49	TBT-AR	2015/04/02	COMPAL	AR PD DEBUG	Add @RT236, RT237	0.3 (X02)
32	47	TBT-AR	2015/04/02	COMPAL	Follow CRB0.998	change UT2.R13 to +3.3V TBT_L,add CT203,CT204,LT2.change CT129,CT130,CT131 to 47uF,remove CT132	0.3 (X02)
33	36	MEC5085	2015/04/03	COMPAL	Change Board ID to X02	Change RE79 to 33K ohm	0.3 (X02)
34	20, 31	LAN SMBUS	2015/04/07	COMPAL	+3.3V_ALW_PCH and +3.3V_RUN backdrive EA	Pop RH67, RH77; Depop RC19, RC20	0.3 (X02)
35	33	JSIM1	2015/04/07	COMPAL	ME CONN	Change footprint to T-SOL_5-991503004000-6_8P-T	0.3 (X02)
36	33	JTHB1	2015/04/07	COMPAL	ME CONN	Change footprint to JAE_DX07B024XJ1R1100_24P-T	0.3 (X02)
37	25	HDMI	2015/04/08	COMPAL	HDMI EA	Depop RV302, RV654, RV683-RV693; Pop LV3, LV6, LV9, LV12, RV207	0.3 (X02)
38	25	HDMI	2015/04/08	COMPAL	HDMI EA	Remove RV654, RV683, RV684, RV685	0.3 (X02)
39	48	TBT-AR	2015/04/09	COMPAL	AR LDO PWR EN ADD Cap	Add CT205 & Depop	0.3 (X02)
40	26	PS8349B	2015/04/10	COMPAL	E-DOCK DP Port1 can't display	Add RV1102 CPU_DP1_AUXN_C 1M pull high +3.3V_RUN	0.3 (X02)
41	21	GPU PWR EN	2015/04/13	COMPAL	GPU lost intermittently	Pop RH346, Depop RH349	0.3 (X02)
42	35, 51	GPU_PWR_LEVEL	2015/04/13	COMPAL	GPIO[A7] (GPU_PWR_LEVEL) need to seeting to PF, so we can de-pop RV113,RE304.	Depop RV113, RE304	0.3 (X02)
43	41	DOCK_DP_HPD	2015/04/13	COMPAL	Depop DOCK DP HPD PD resistor for PS8349B/PS8348B internal PD.	Depop R268, R271	0.3 (X02)

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44	43	PAD & ME & LED	2015/04/14	COMPAL	JSIM1 CONN 2nd JAE	JSIM1 CONN 2nd JAE	0.4 (X03)
45	33	SIM Detect	2015/04/14	COMPAL	Add SIM Detect for Hot Plug	Add RI31 for SIM Detect	0.4 (X03)
46	35	EC	2015/04/20	COMPAL	Align PC U & H GPIO for EC common code	Add RE311 PU for AR_SMBUS_ALERT#	0.4 (X03)
47	42	KB	2015/04/20	COMPAL	Add PU for I2C TP Module	Add RZ116, RZ117	0.4 (X03)
48	26,27	Parade DeMux	2015/04/20	COMPAL	Vendor Parade suggest Parade DeMux ouput to Parade Redriver no need AUX PD/PU	Depop RV604, RV608, RV701, RV712	0.4 (X03)
49	46	TBT AR	2015/04/23	COMPAL	For layout space	Remove RT149, RT166	0.4 (X03)
50	46	TBT AR	2015/04/24	COMPAL	Follow Intel AR Reference	Change CT129~CT131 from 47u to 10u. Add CT206 10u	0.4 (X03)
51	49	TBT AR	2015/04/29	COMPAL	CONN Impact Type C return loss	Change JTHB1 from Hybrid to SMD type	0.4 (X03)
52	42	KB_TP	2015/05/05	COMPAL	TP function sometimes lag	CZ30, CZ31 change from 10p to 330p improve signal quality	0.5 (X03)
53	40	USB Charger	2015/05/05	COMPAL	Insert USB HDD Shut Down Issue	Add CI32 Poly 150U	0.5 (X03)
54	36	MEC5085	2015/05/05	COMPAL	AR no function at AC S5	UPD_GPU_SMBDAT/UPD_GPU_SMBCLK PU change from +3.3V_RUN to +3.3V_ALW	0.5 (X03)
55	38	M2280	2015/05/26	COMPAL	Insert NVME SATA LED no function	JNGFF3.10 connected to PCH_SATA_LED#	0.5 (X03)
56	35	EC	2015/05/26	COMPAL	For Type-C function	1. Add 5048 GPIO(PROCHOT_GATE) and reserve RE313 pull high 2. Add 5048(PD_ACE_DET#) for AR config? and pull high on RE312, PD ON RE314	0.5 (X03)
57	22	PCH(7/9)	2015/06/01	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	1.Add RC349 and CC310 on VCCHDA 2.Add RC350 and CC311 on VCCAPLL_1P0	0.5 (X03)
58	47	TBT AR	2015/06/01	COMPAL	AR IC PWR different by version	Add LT3	0.5 (X03)
59	47	TBT AR	2015/06/09	COMPAL	PWR Consumption measurement	Add PJP41, PJP42	0.5 (X03)
60	47	TBT AR	2015/06/09	COMPAL	ESD	Reserve DT25~DT28	0.5 (X03)
61	51	GPU	2015/06/10	COMPAL	For AR SMBUS	Depop QV14	0.5 (X03)
62	25	HDMI	2015/06/11	COMPAL	Remove HDMI choke	Add RV683, RV684, RV685, RV654; Pop RV686, RV687, RV688, RV689, RV690, RV691, RV692, RV693; Depop LV3, LV6, LV9, LV12; Change RV303 from 4.99K to 4.02K	0.5 (X03)
63	26, 27	*	2015/06/11	COMPAL	Dell recommend	Change RE312 from 100K to 330K Reserve CV1104, CV1105 for SW1_DP1_HPD & SW2_DP1_HPD	0.5 (X03)
64	35	EC	2015/06/11	COMPAL	PROCHOT_GATE default PD	Add RE315 PD 100K	0.5 (X03)
65	36	EC	2015/06/11	COMPAL	Win PE Global Reset Issue	Add QE11	0.6 (X04)
66	36	EC	2015/06/11	COMPAL	Intel Sequence Fail	Add UE5	0.6 (X04)

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